

B550 AORUS MASTER

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[illegible]

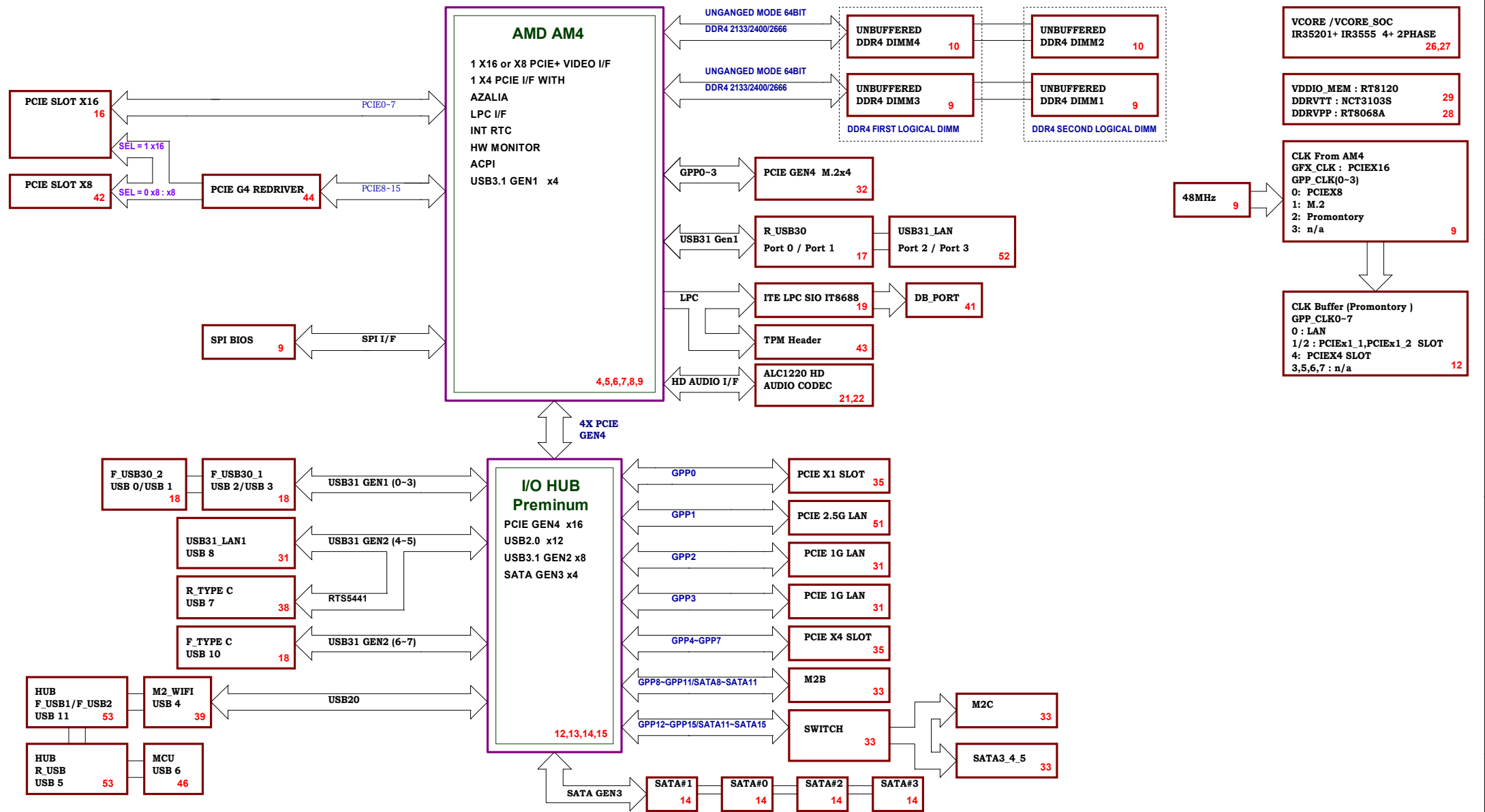
5	4	3	2	1
---	---	---	---	---

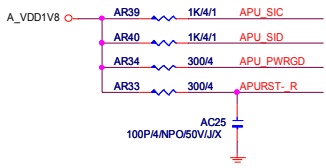
P-Code: U98126-0

	SPI_CLK	LFRAME-	SYS_RST-	LPC_CLK0	LPC_CLK1
PULL HIGH	Internal clock mode	SPI ROM	Normal reset mode	PSP modify SPI page reg bits[24:24]	Use 48MHz crystal clock
PULL LOW	Extal clock mode	LPC ROM	Short reset mode	PSP not modify SPI page reg bits[24:24]	Use 100MHz extl clock input.

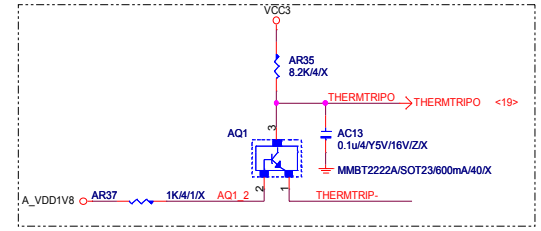
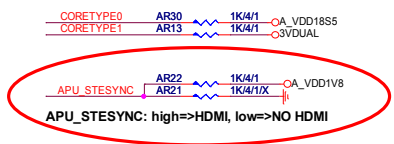
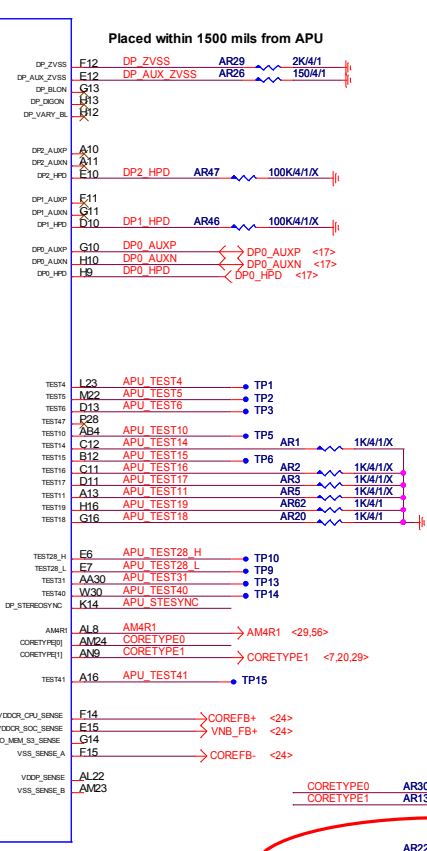
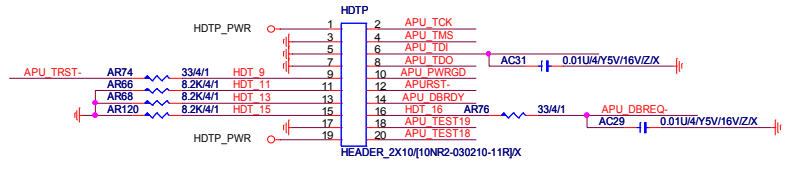
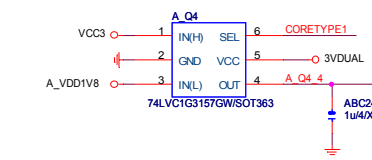
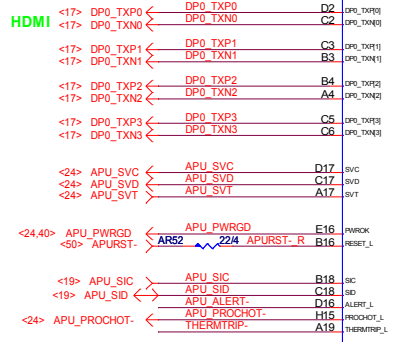
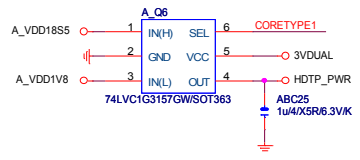
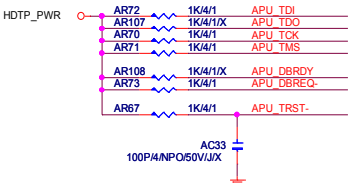
[illegible]

			
Title			
<div style="text-align: center;"> BOM & PCB HISTORY </div>			
Size	Custom	Document Number	Rev
		<div style="text-align: center;"> B550 AORUS MASTER </div>	<div style="text-align: center;"> 1.01 </div>
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SVC	SVD	Boot voltage
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



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CORETYPE 1	CORETYPE 0	Family / Model Numbers	AM4 APU TYPE
0 BR	0	Family 15 h / Models 60 h-6 Fh	TYPE 0
0 ST	1	Reserved	TYPE 1
1 ZP	0	Family 17 h / Models 00 h-0 Fh	TYPE 2
1 RV	1	Family 17 h / Models 10 h-1 Fh	TYPE 3

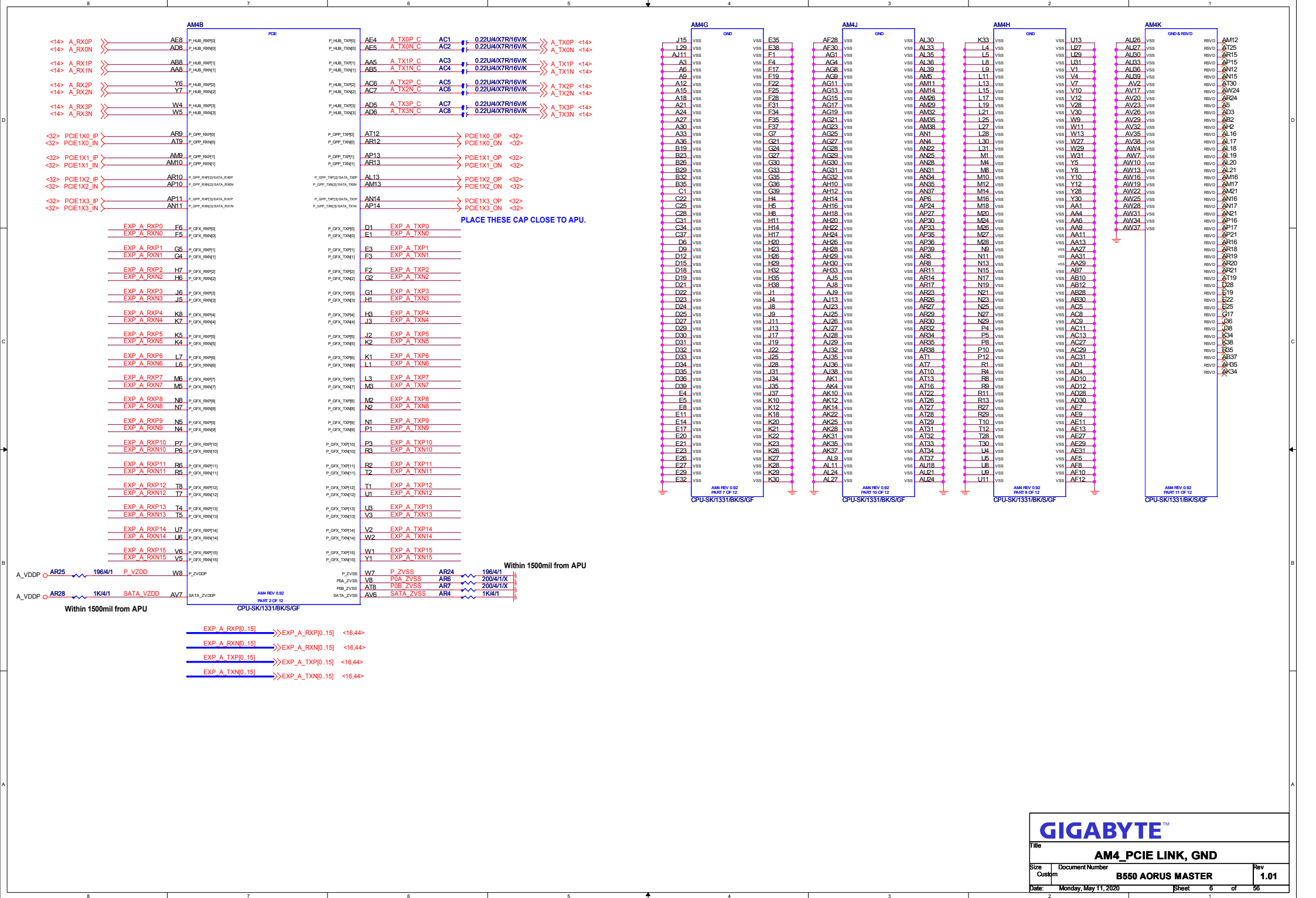
GIGABYTE

Title: **CPU CONTROL**

Size: **B550 AORUS MASTER**

Rev: **1.01**

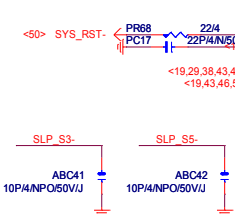
Date: Monday, May 11, 2020



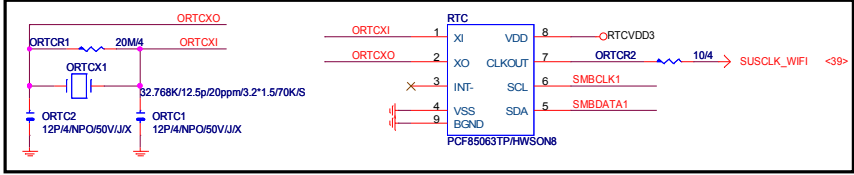
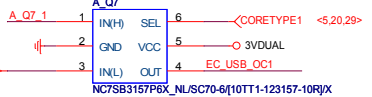
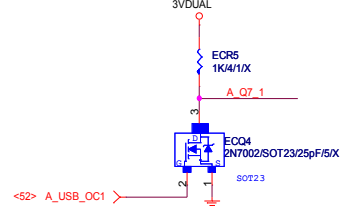
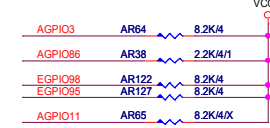
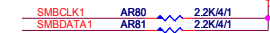
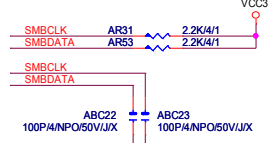
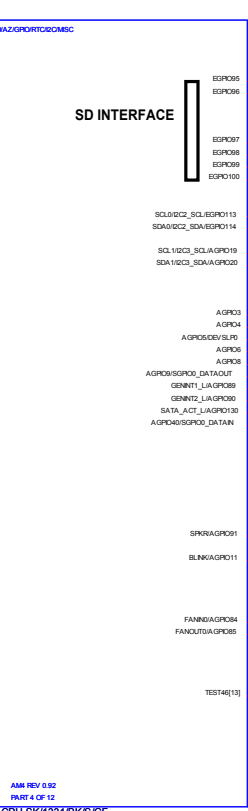
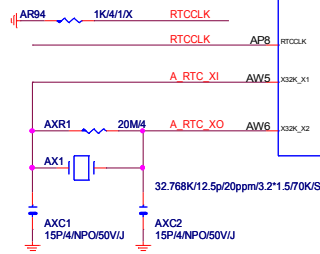
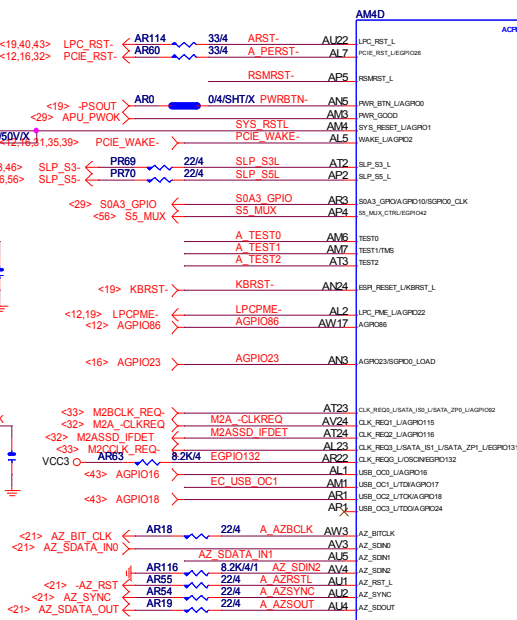
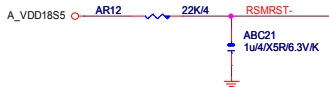
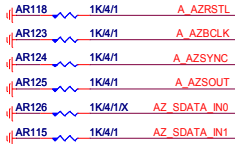
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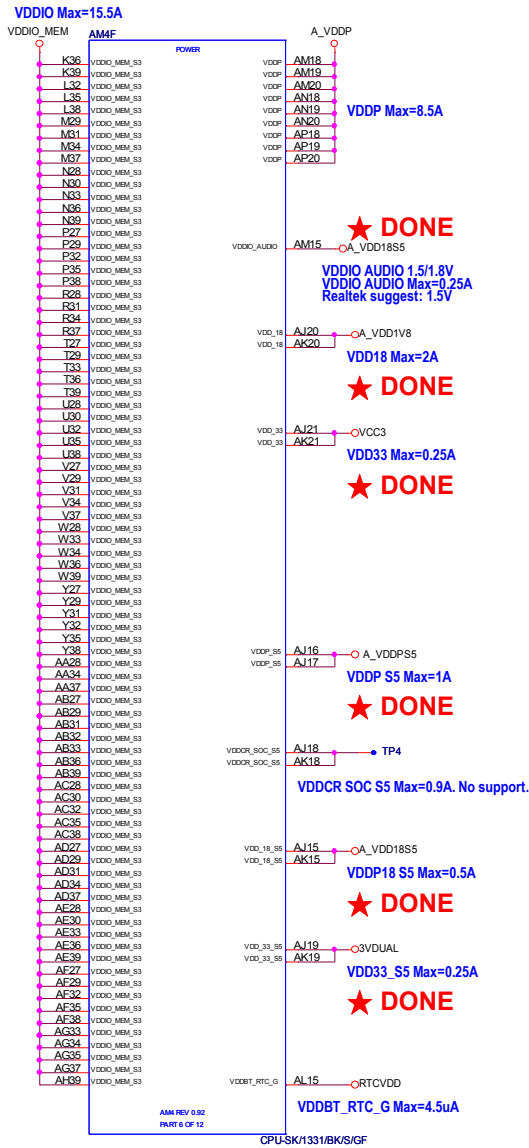
AM4_PCIE LINK, GND

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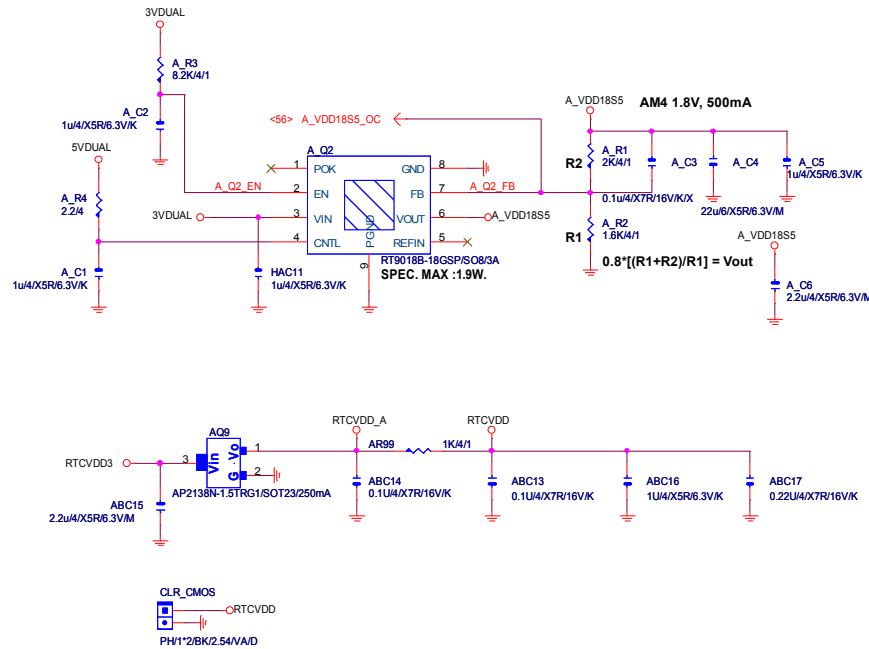


TEST0	TEST1	TEST2	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserve
0	1	X	Reserve
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on JTAG only, Yuba JTAG enable.



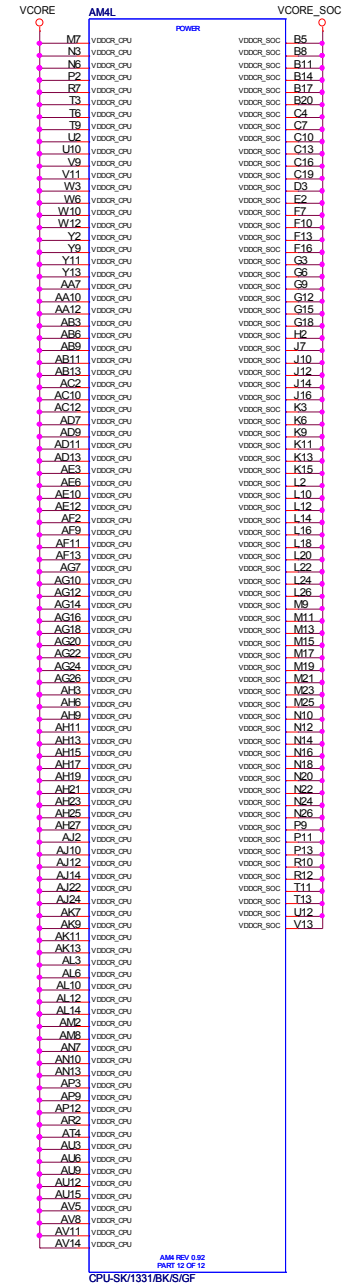


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Vcore EDC =15.5A
Vcore 0.75~1.5V

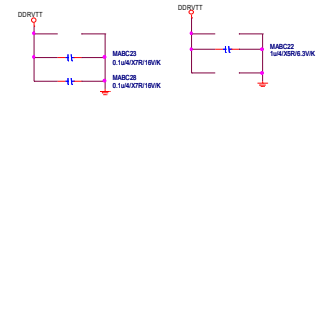
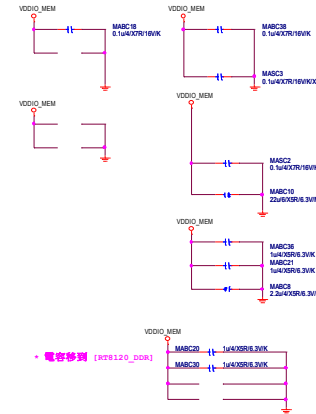
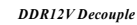
Vcore EDC =75A
Vcore SOC 0.75~1.2V

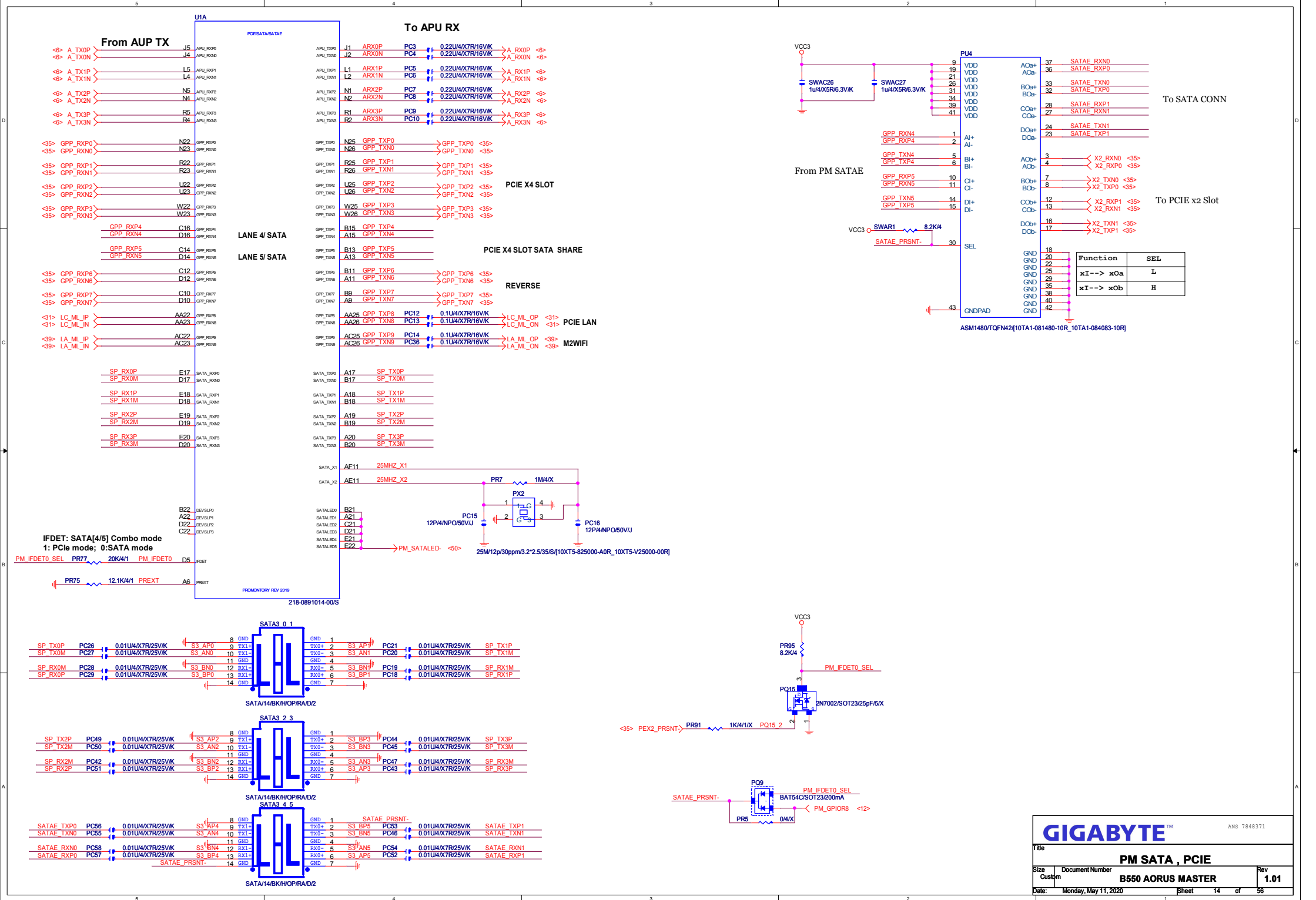


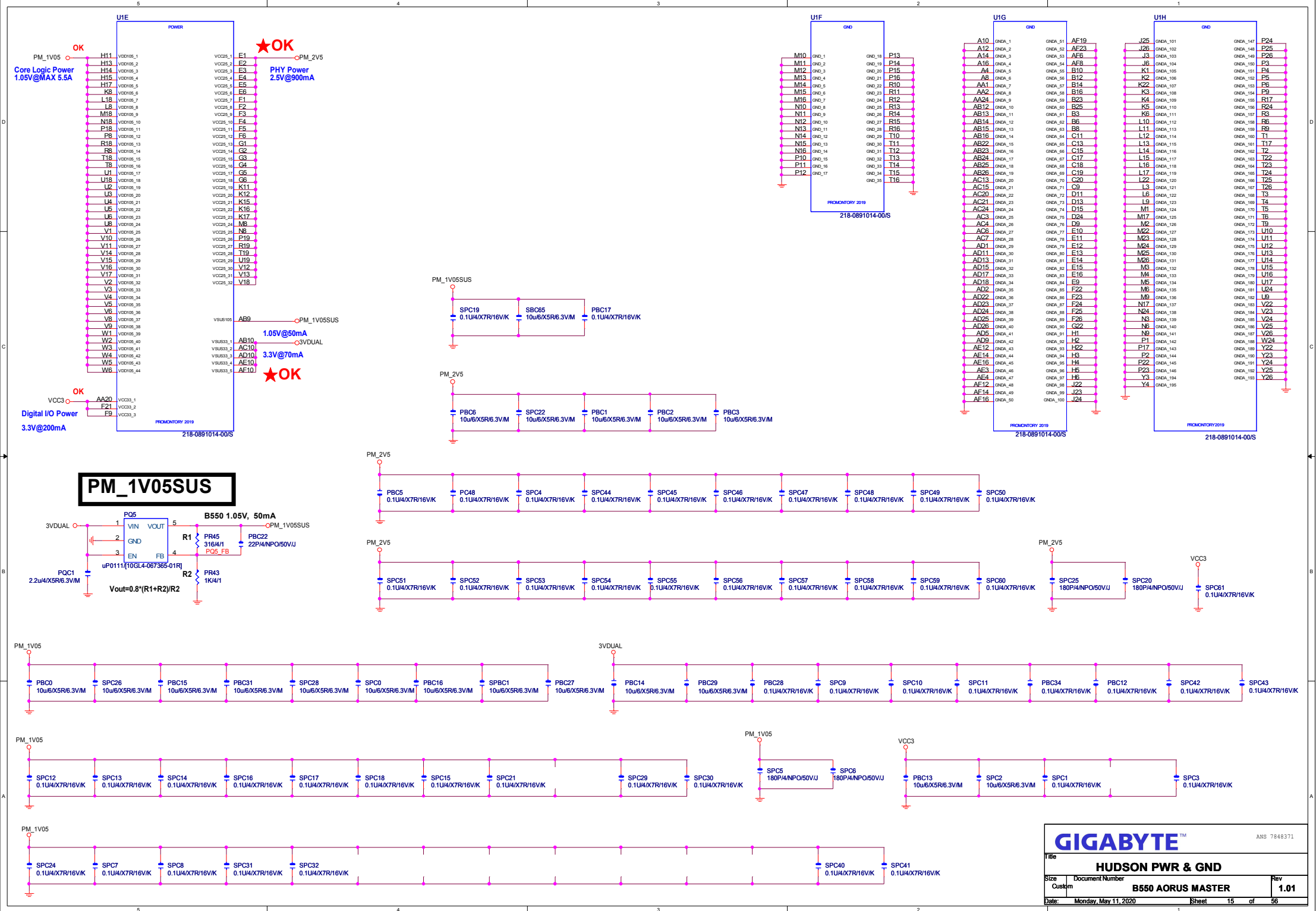


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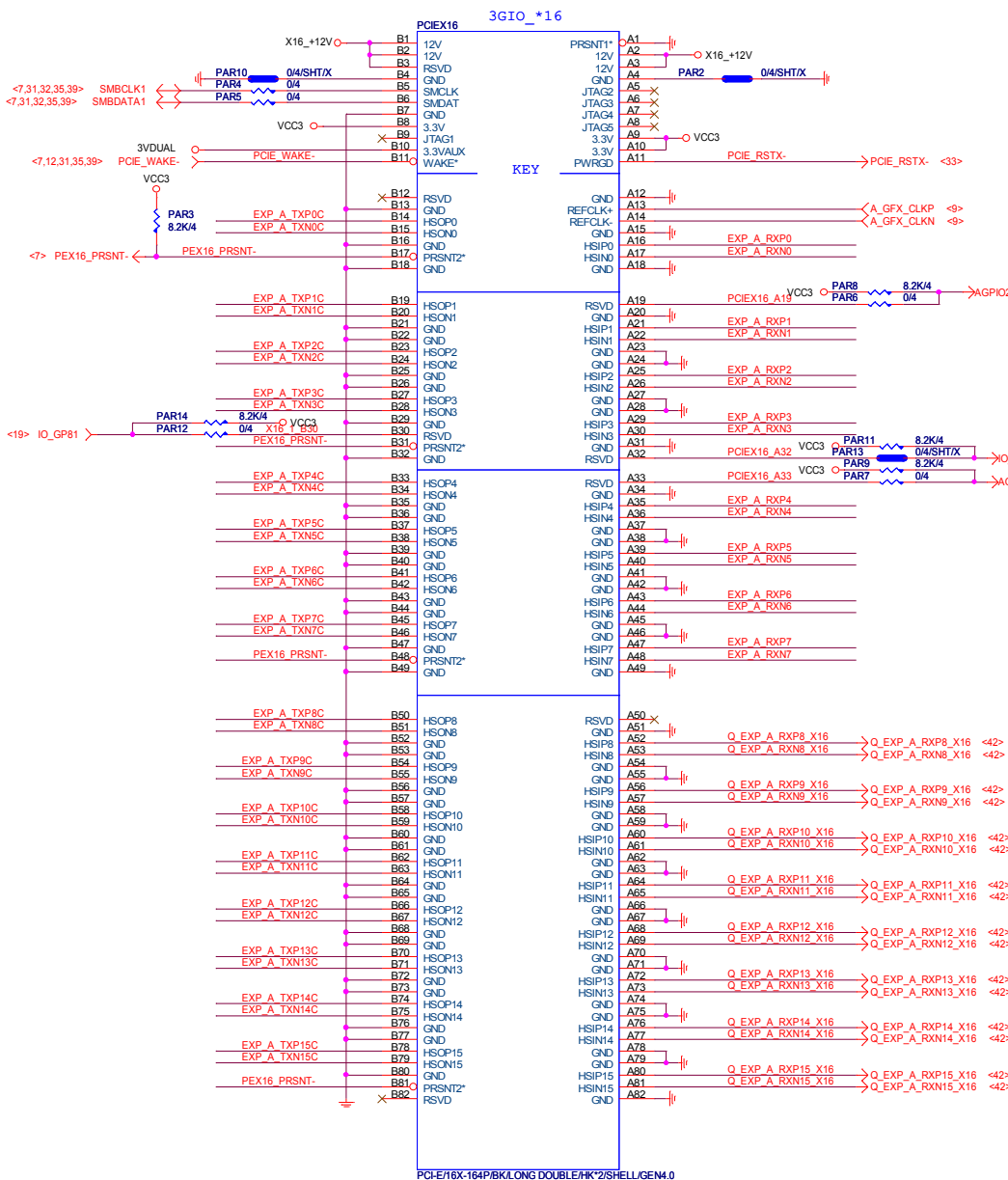
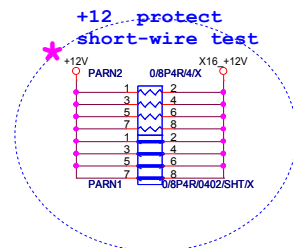






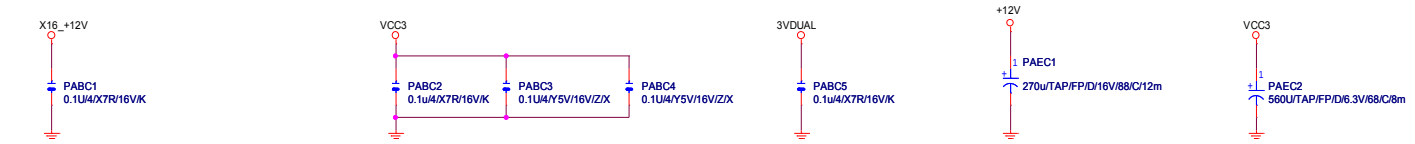


EXP_A_RXP[0..7] >> EXP_A_RXP[0..7] <&6>
EXP_A_RXN[0..7] >> EXP_A_RXN[0..7] <&6>
<&6> EXP_A_TXP[0..7] >> EXP_A_TXP[0..7]
<&6> EXP_A_TXN[0..7] >> EXP_A_TXN[0..7]



A19, A33 config address/ detect.(AGPIO23, AGPIO9)
B30 low config 4 x4. (IO_GP81) Hank card.4XM2G4
A32 low, default. (IO_GP82) Sam card

EXP_A_TXP0	PAC4	0.22u4/X5R6.3V/K	EXP_A_TXP0C
EXP_A_TXN0	PAC5	0.22u4/X5R6.3V/K	EXP_A_TXN0C
EXP_A_TXP1	PAC6	0.22u4/X5R6.3V/K	EXP_A_TXP1C
EXP_A_TXN1	PAC7	0.22u4/X5R6.3V/K	EXP_A_TXN1C
EXP_A_TXP2	PAC8	0.22u4/X5R6.3V/K	EXP_A_TXP2C
EXP_A_TXN2	PAC9	0.22u4/X5R6.3V/K	EXP_A_TXN2C
EXP_A_TXP3	PAC10	0.22u4/X5R6.3V/K	EXP_A_TXP3C
EXP_A_TXN3	PAC11	0.22u4/X5R6.3V/K	EXP_A_TXN3C
EXP_A_TXP4	PAC12	0.22u4/X5R6.3V/K	EXP_A_TXP4C
EXP_A_TXN4	PAC13	0.22u4/X5R6.3V/K	EXP_A_TXN4C
EXP_A_TXP5	PAC14	0.22u4/X5R6.3V/K	EXP_A_TXP5C
EXP_A_TXN5	PAC15	0.22u4/X5R6.3V/K	EXP_A_TXN5C
EXP_A_TXP6	PAC16	0.22u4/X5R6.3V/K	EXP_A_TXP6C
EXP_A_TXN6	PAC17	0.22u4/X5R6.3V/K	EXP_A_TXN6C
EXP_A_TXP7	PAC18	0.22u4/X5R6.3V/K	EXP_A_TXP7C
EXP_A_TXN7	PAC19	0.22u4/X5R6.3V/K	EXP_A_TXN7C
EXP_A_TXP8	PAC20	0.22u4/X5R6.3V/K	EXP_A_TXP8C
EXP_A_TXN8	PAC21	0.22u4/X5R6.3V/K	EXP_A_TXN8C
EXP_A_TXP9	PAC22	0.22u4/X5R6.3V/K	EXP_A_TXP9C
EXP_A_TXN9	PAC23	0.22u4/X5R6.3V/K	EXP_A_TXN9C
EXP_A_TXP10	PAC24	0.22u4/X5R6.3V/K	EXP_A_TXP10C
EXP_A_TXN10	PAC25	0.22u4/X5R6.3V/K	EXP_A_TXN10C
EXP_A_TXP11	PAC26	0.22u4/X5R6.3V/K	EXP_A_TXP11C
EXP_A_TXN11	PAC27	0.22u4/X5R6.3V/K	EXP_A_TXN11C
EXP_A_TXP12	PAC28	0.22u4/X5R6.3V/K	EXP_A_TXP12C
EXP_A_TXN12	PAC29	0.22u4/X5R6.3V/K	EXP_A_TXN12C
EXP_A_TXP13	PAC30	0.22u4/X5R6.3V/K	EXP_A_TXP13C
EXP_A_TXN13	PAC31	0.22u4/X5R6.3V/K	EXP_A_TXN13C
EXP_A_TXP14	PAC32	0.22u4/X5R6.3V/K	EXP_A_TXP14C
EXP_A_TXN14	PAC33	0.22u4/X5R6.3V/K	EXP_A_TXN14C
EXP_A_TXP15	PAC34	0.22u4/X5R6.3V/K	EXP_A_TXP15C
EXP_A_TXN15	PAC35	0.22u4/X5R6.3V/K	EXP_A_TXN15C



GIGABYTETM

PCI EXPRESS X 16

Size

Document Number

Rev

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B550 AORUS MASTER

1.01

Date

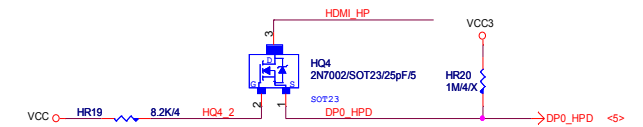
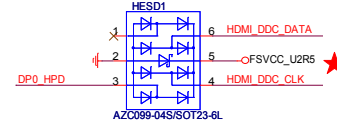
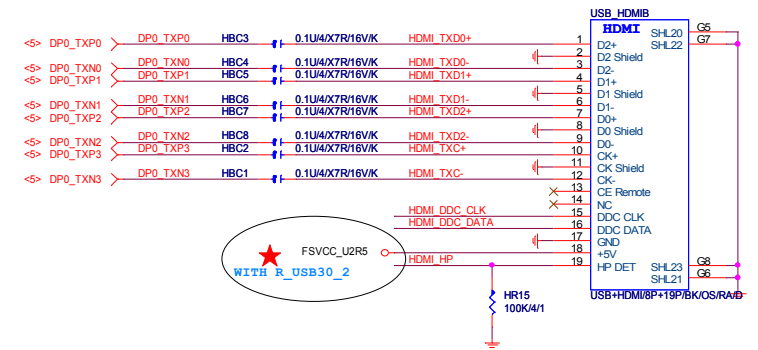
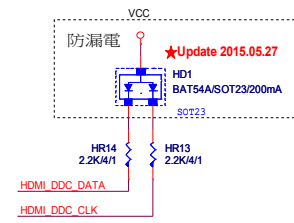
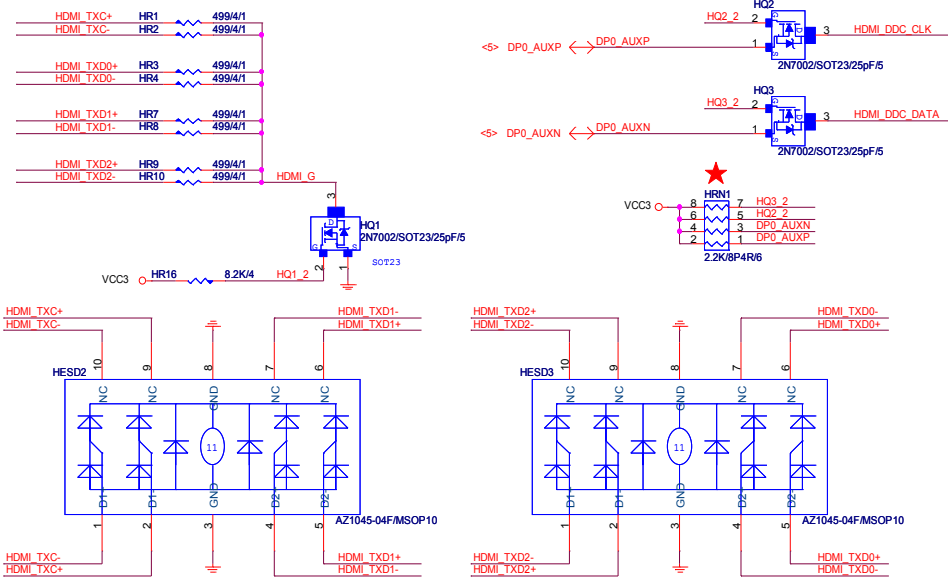
Monday, May 11, 2020

Sheet

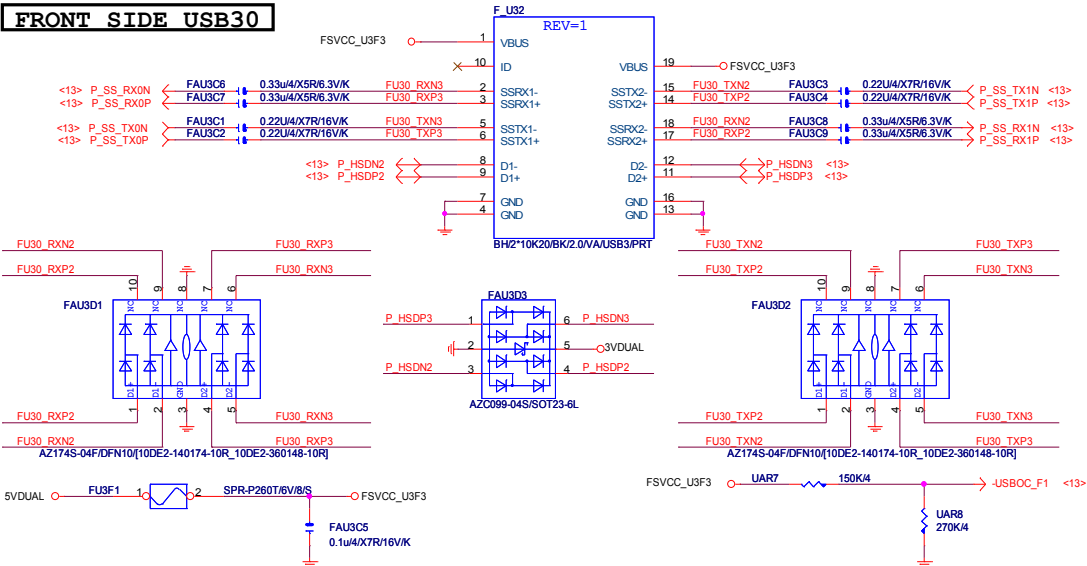
16

of

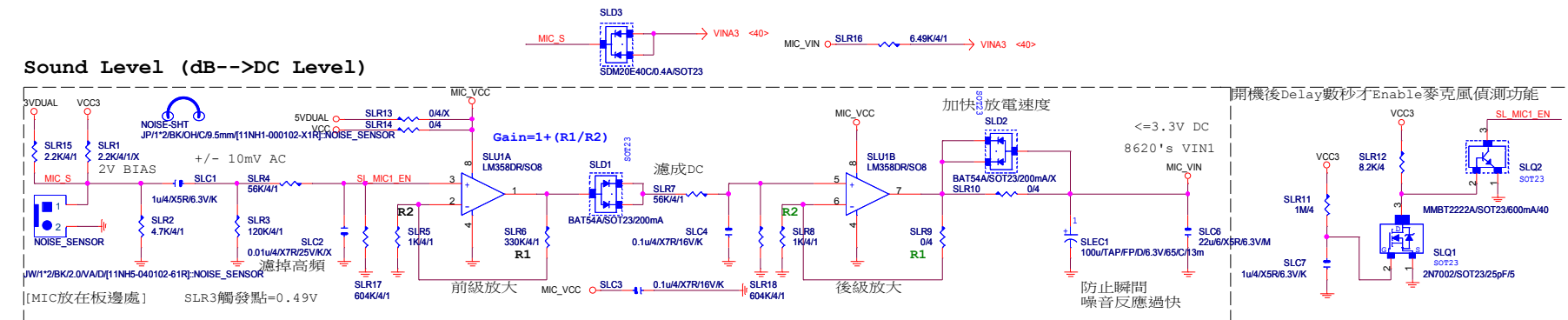
56



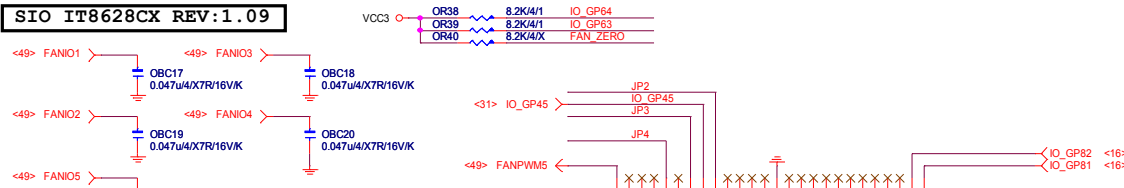
FRONT SIDE USB30



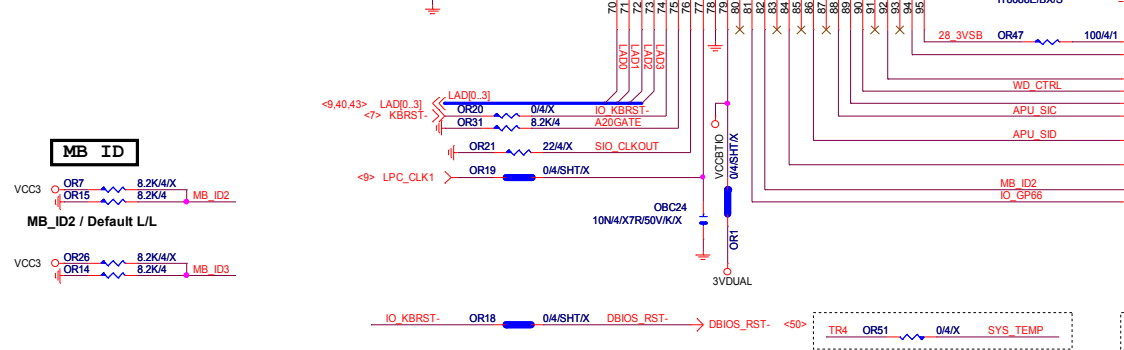
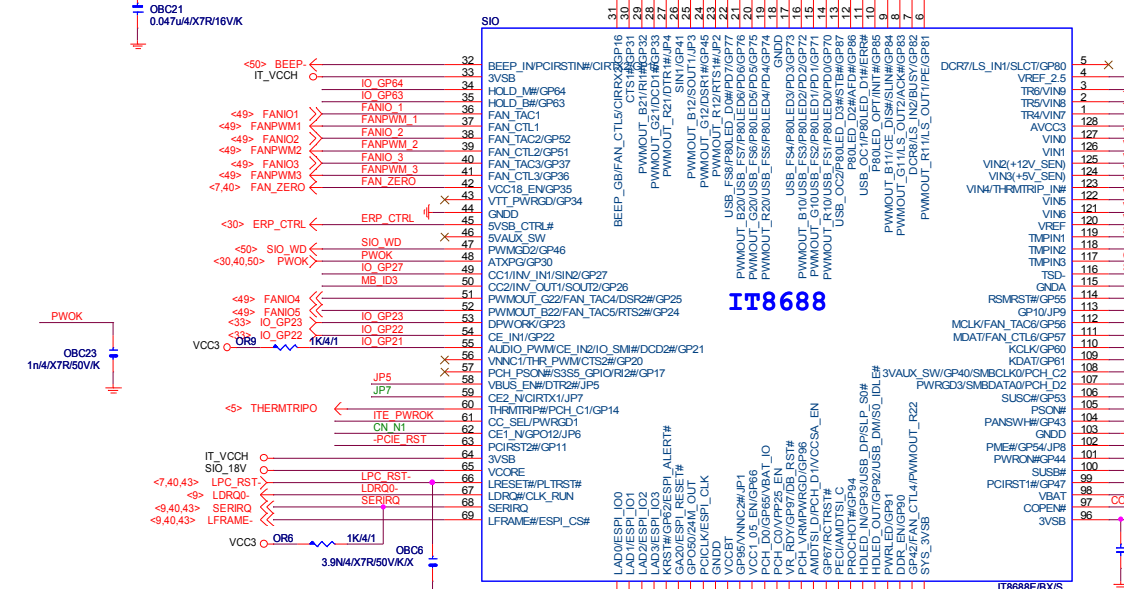
Sound Level (dB-->DC Level)



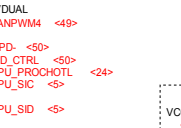
SIO IT8628CX REV:1.09



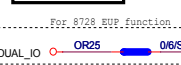
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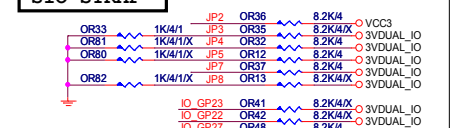
EUP control detect



PWR SHT

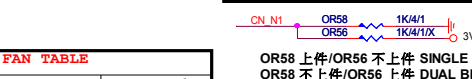


SIO STRAP



JP2	1	Disable WDT to rest PWROK
	0	Enable WDT to rest PWROK
JP3		Dual-BIOS CS pin mode select bit "0"
		See the below table
JP4	1	LPC/ESPI power VCCBT = 3.3V
	0	LPC/ESPI power VCCBT = 1.8V
JP5	1	LPC I/F
	0	ESPI I/F
JP6	1	Enable Dual BIOS Function (for GigaByte Only)
	0	Disable Dual BIOS Function (for GigaByte Only)
JP7		Dual-BIOS CE pin mode select bit "*"
		See the below table
	1 1	CE pin disable (Hold pin mode)
JP7	1 0	CE mode 1
JP3	0 1	CE mode 2
	0 0	CE mode 3

DUAL BIOS OPT STRAP



OR58 上件/OR56 不上件 SINGLE BIOS,
OR58 不上件/OR56 上件 DUAL BIOS

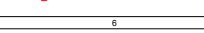
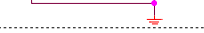
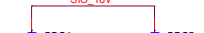
EMI



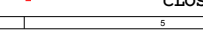
Power leakage

SIO 18V

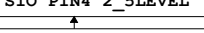
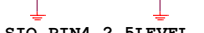
internal power pin, max 22nF cap



SIO CAP



SIO PU



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File

ITE 8686 LPC IO, TPM, KB/MS

Size

Document Number

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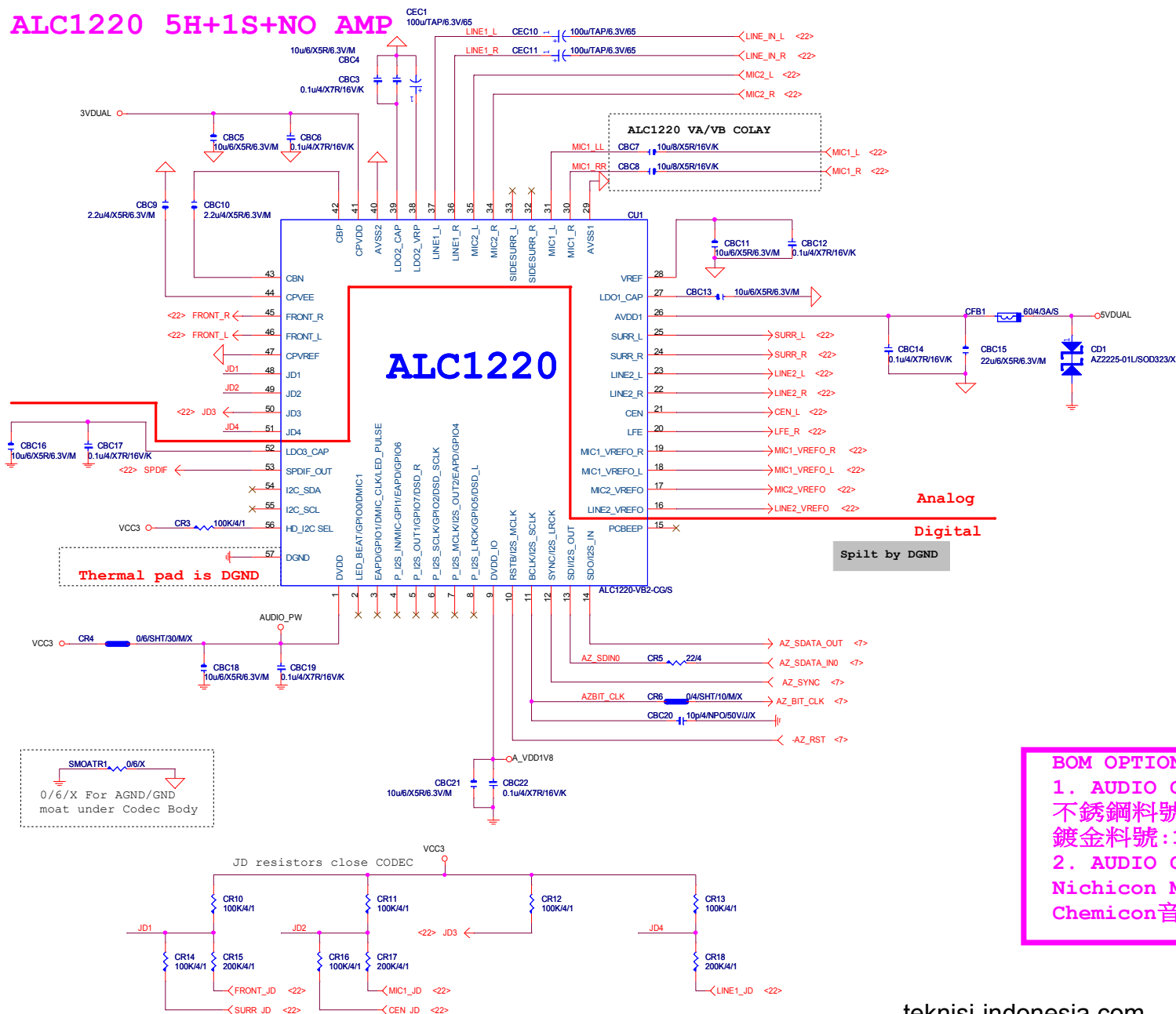
of

56

Rev

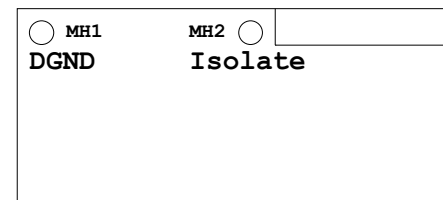
1.01

ALC1220 5H+1S+NO AMP



LAYOUT注意:螺絲孔下GND方式

1. MH1下DGND
2. MH2一律改為Isolate

LAYOUT注意:是否要加?
AGND切割線

BOM OPTION :

1. AUDIO CONNECT

不銹鋼料號:11NR6-403025-A3R

鍍金料號:11NR6-403025-92R

2. AUDIO CAP

Nichicon MW音效電容 : 11CE1-651000-12R

Chemicon音效電容 : 11CE2-651000-05R

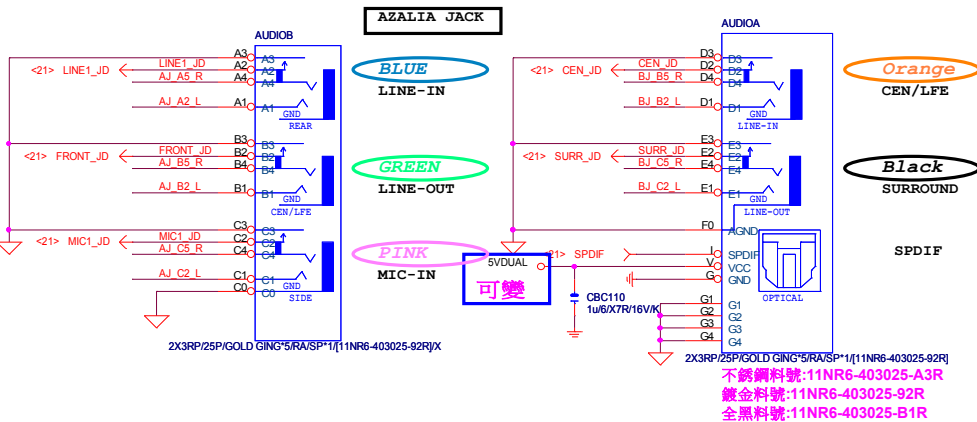
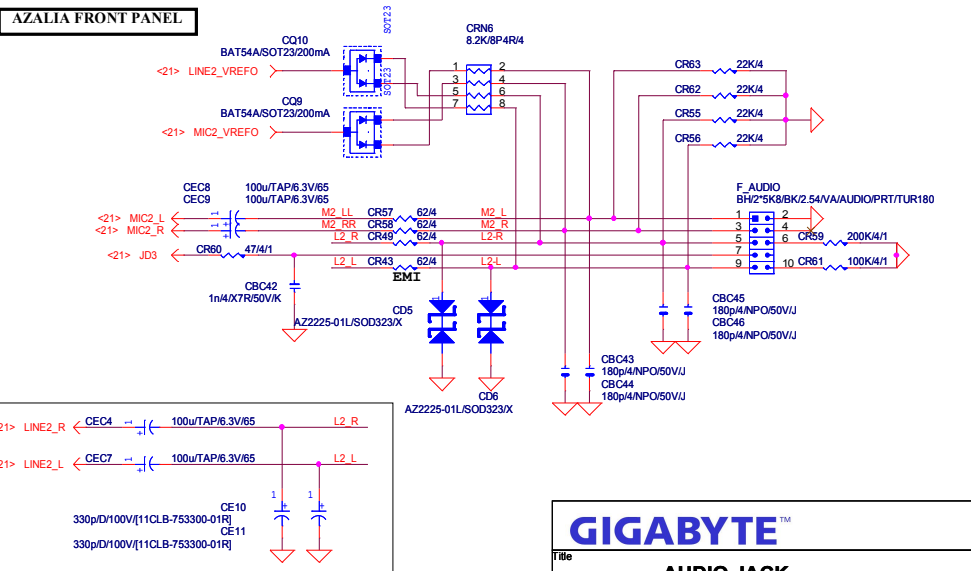
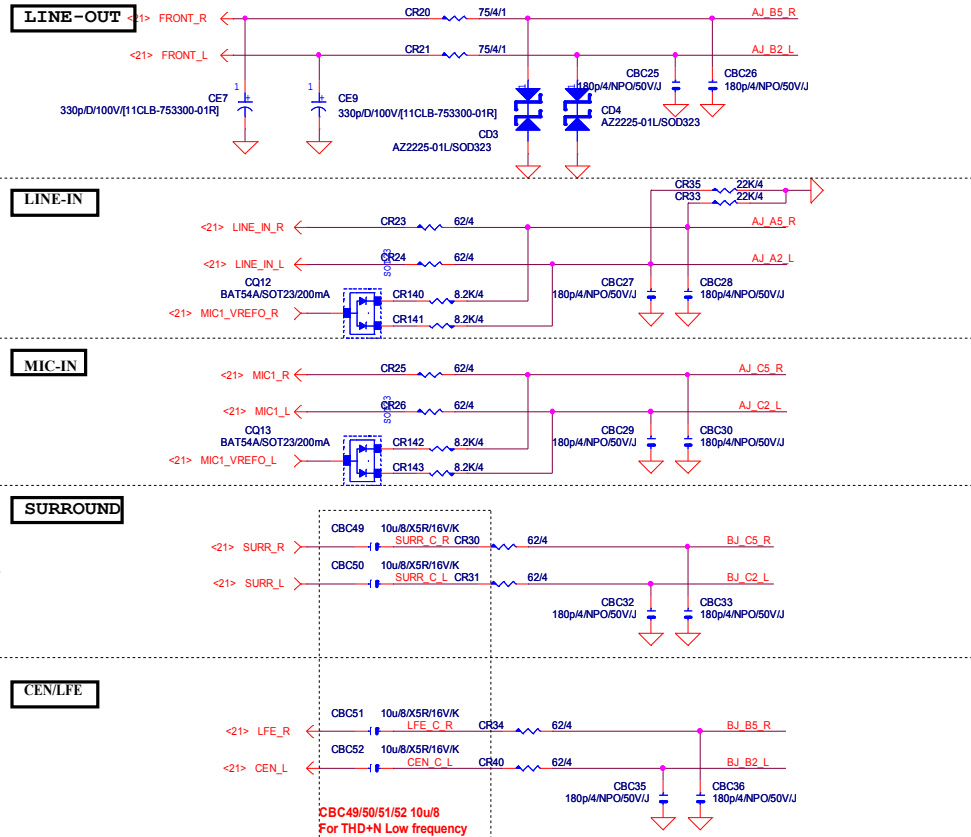
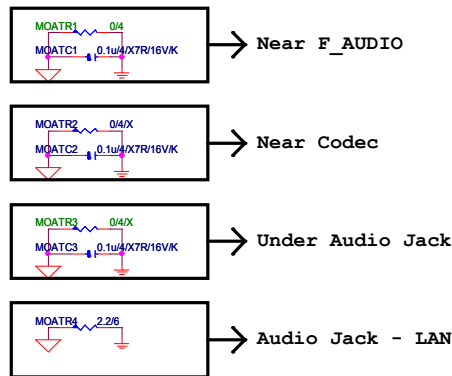
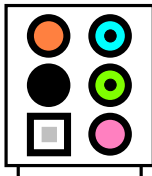
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Title			
ALC1220 REAR			
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Rev 2.05

AZALIA JACK



GIGABYTE

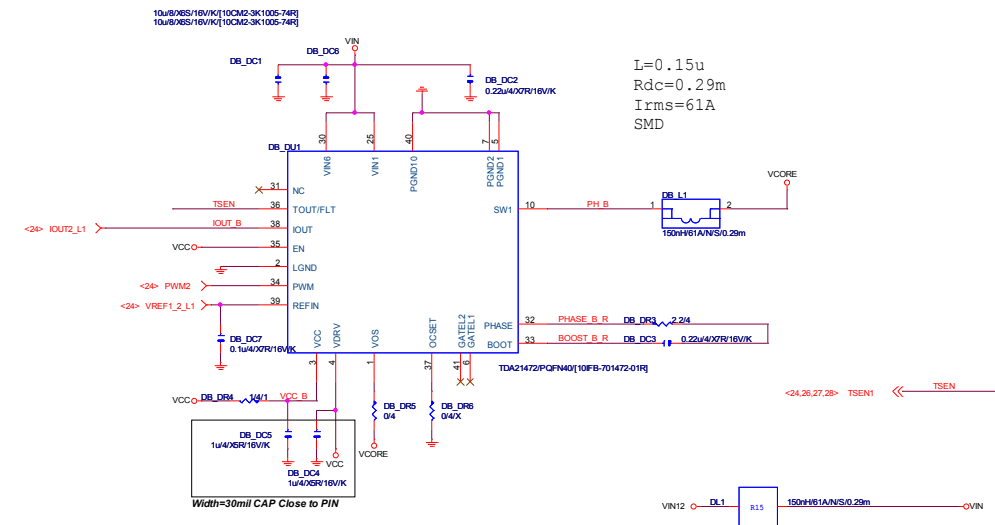
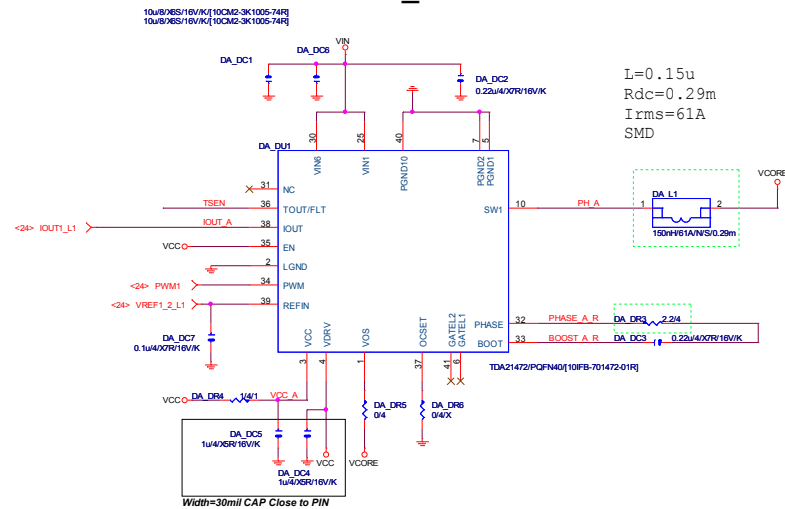
Title			
AUDIO JACK			
Size	Document Number	Rev	
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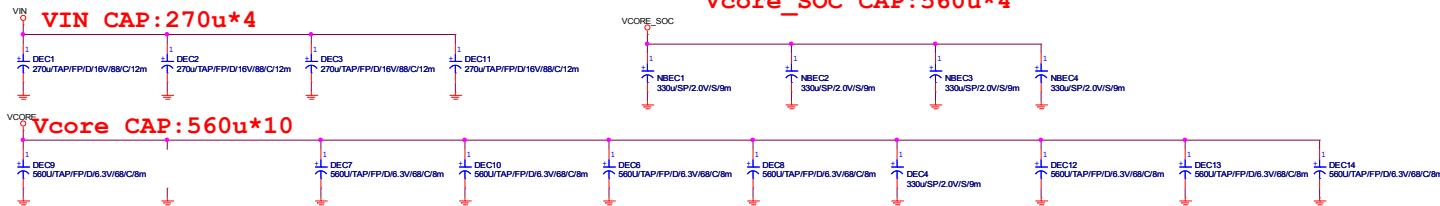
GIGABYTE TM			
Title DIGITAL LED			
Size	Document Number		Rev
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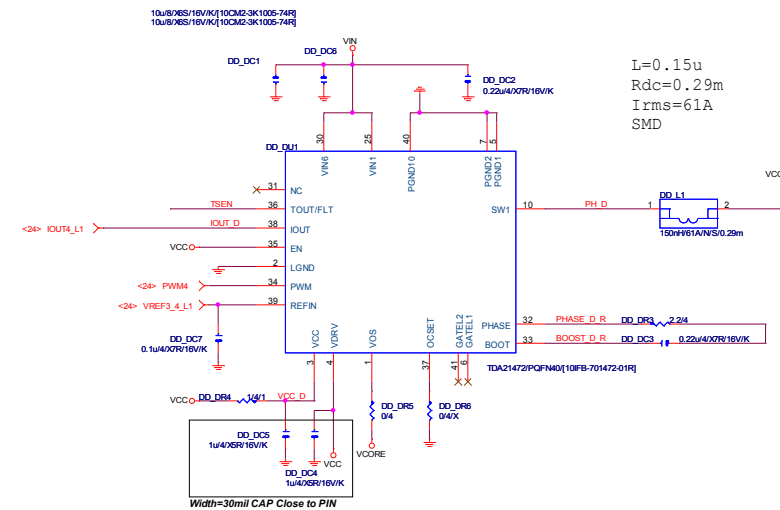
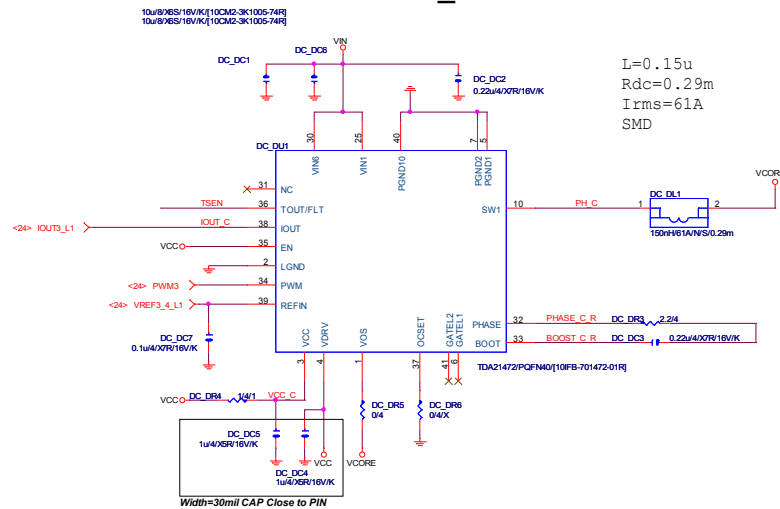
VCORE PHASE1_2



Vcore_SOC CAP:560u*4

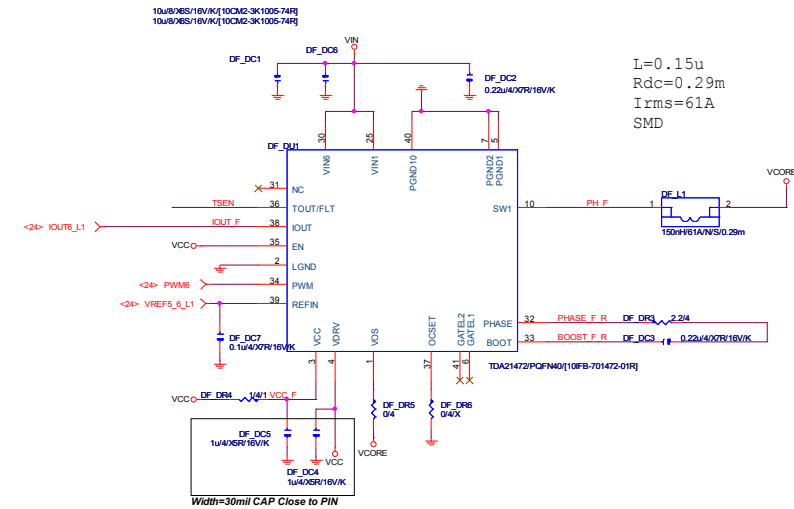
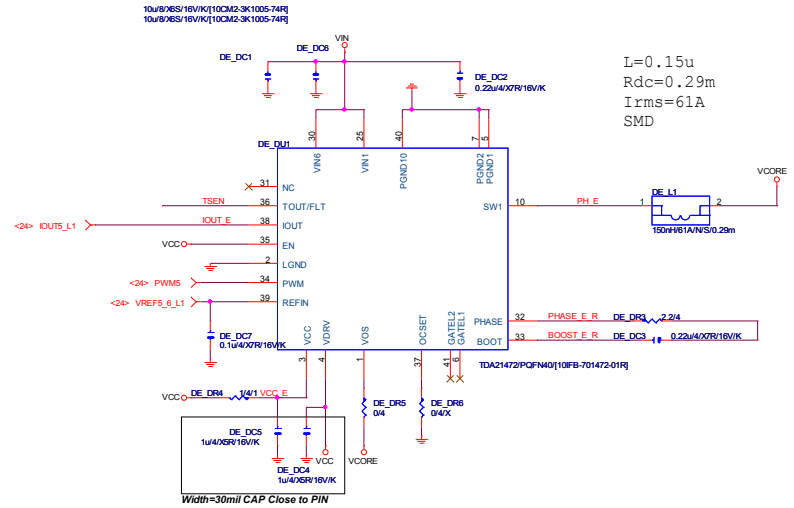


VCORE PHASE3_4



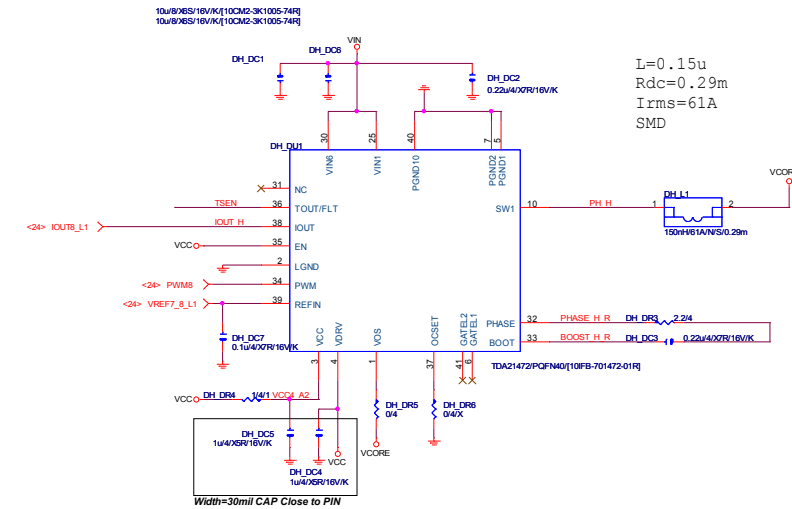
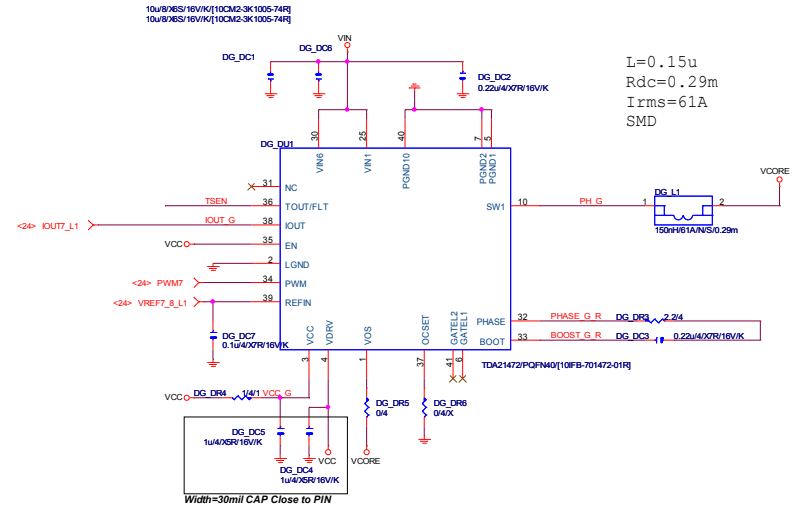
REV:0.11

VCORE PHASE5_6

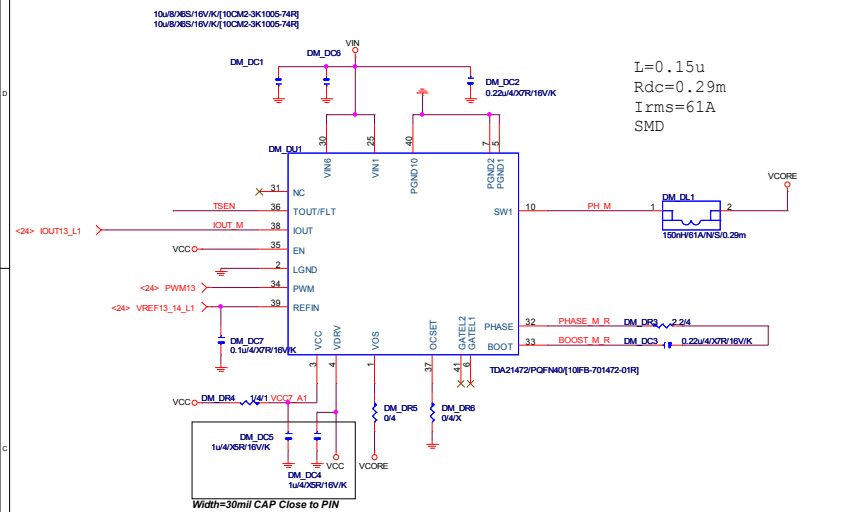


<24,25,27,28> TSEN1 << TSEN

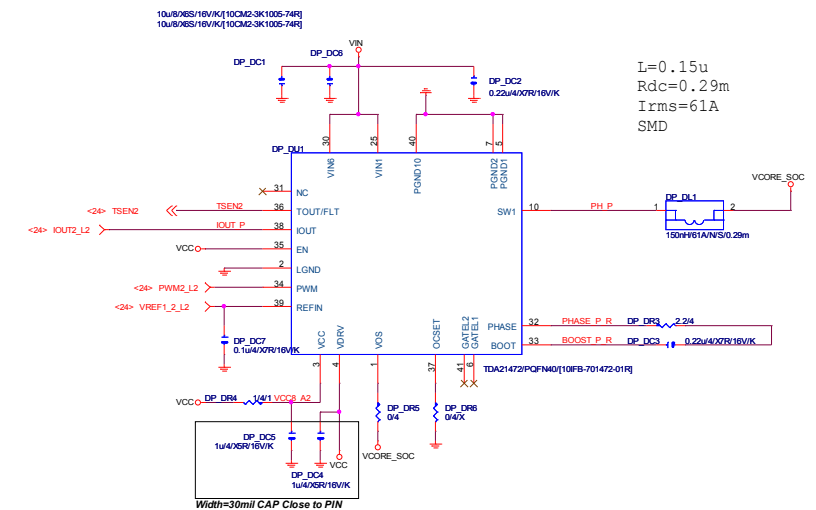
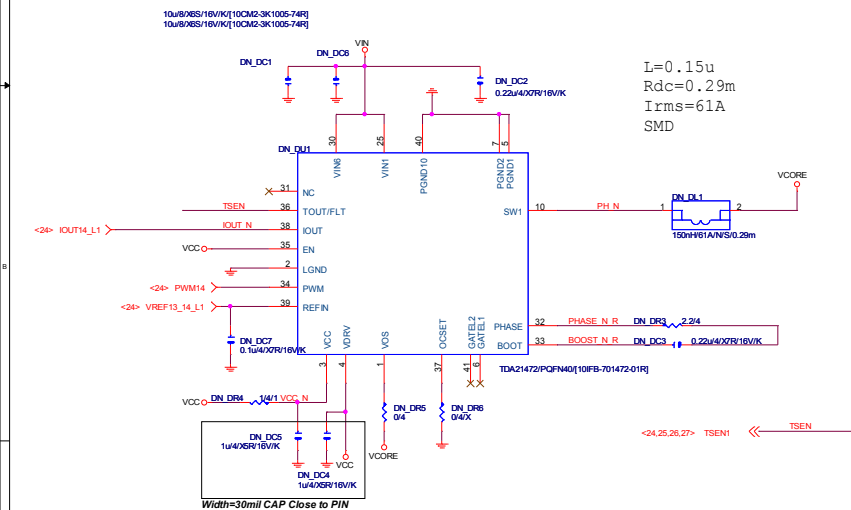
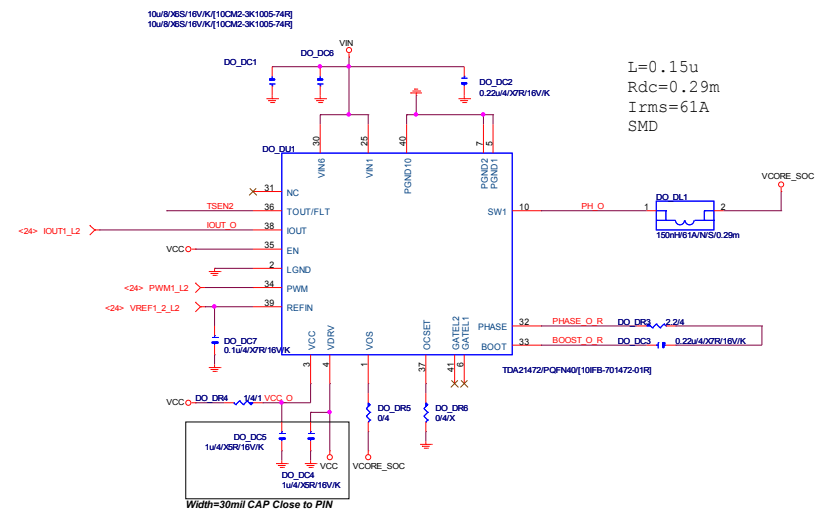
VCORE PHASE7_8



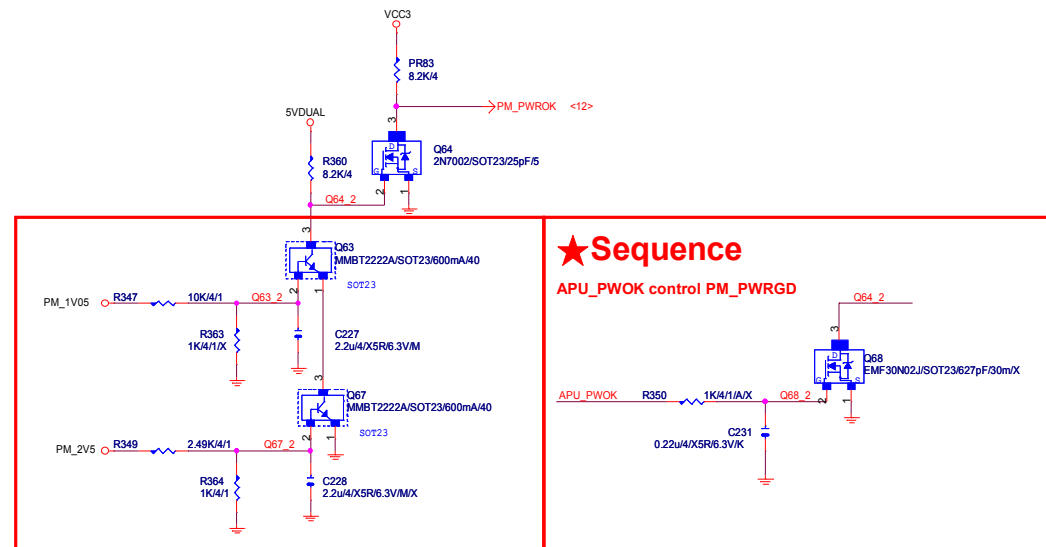
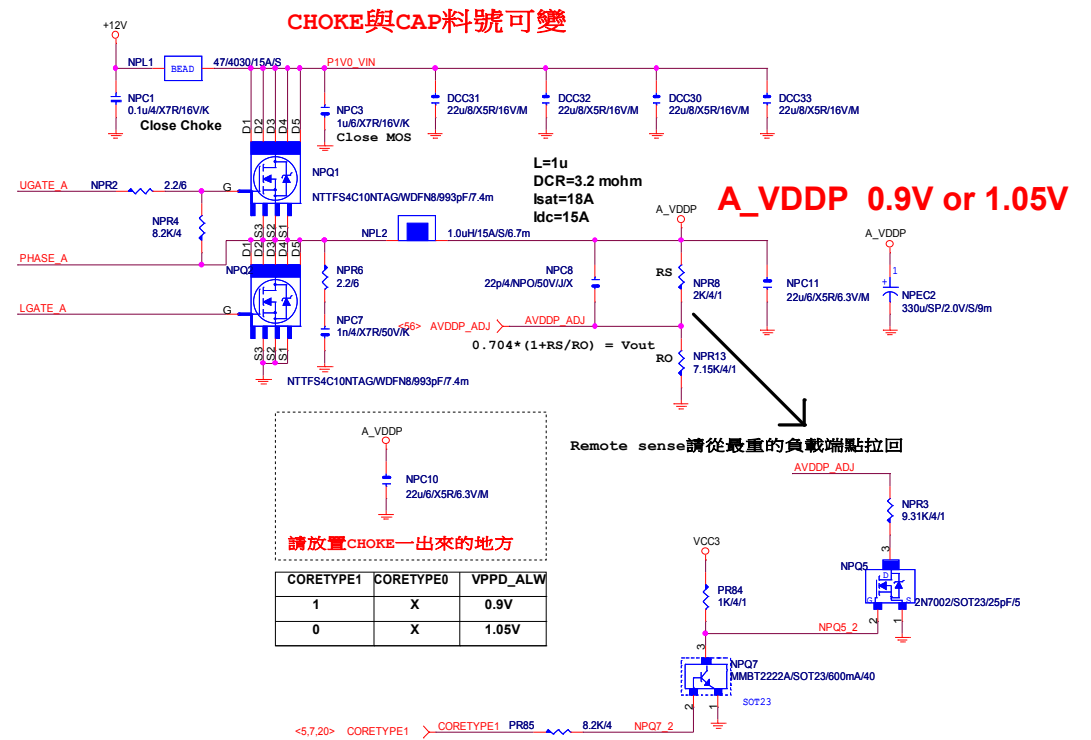
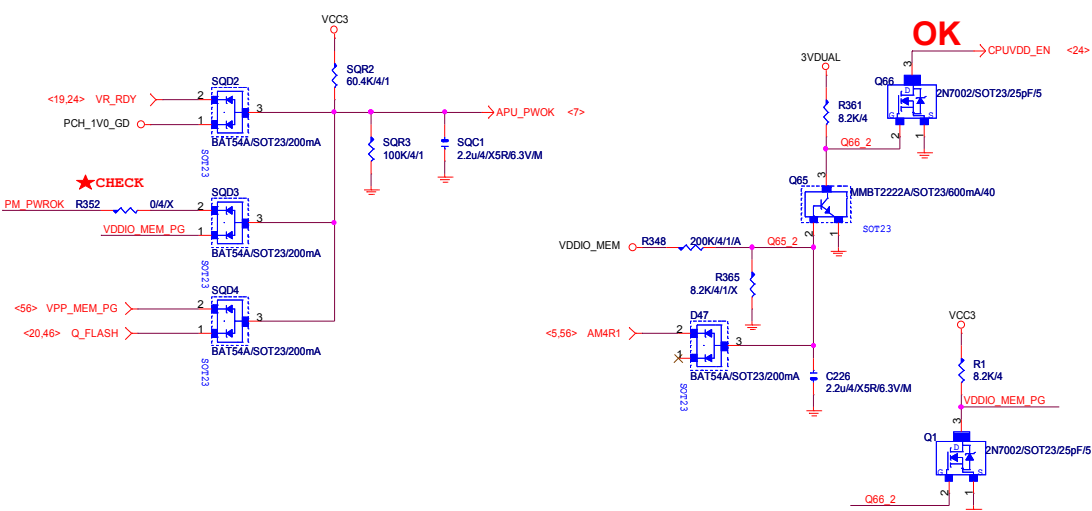
VCORE PHASE13_14

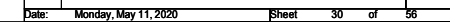
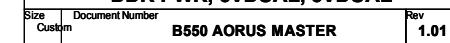
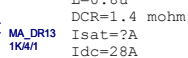
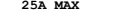
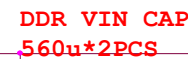
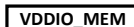


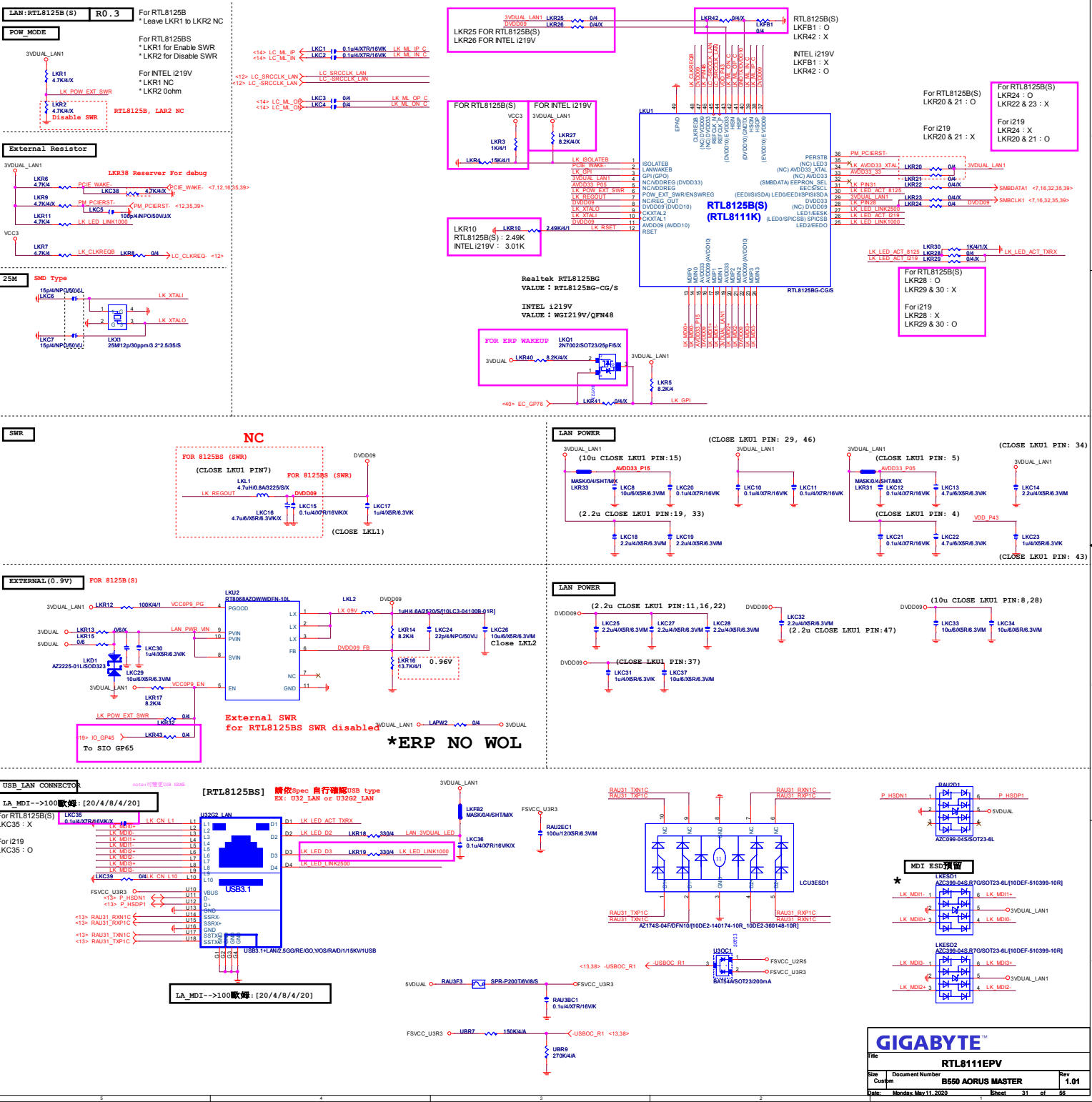
VSOC PHASE1_2



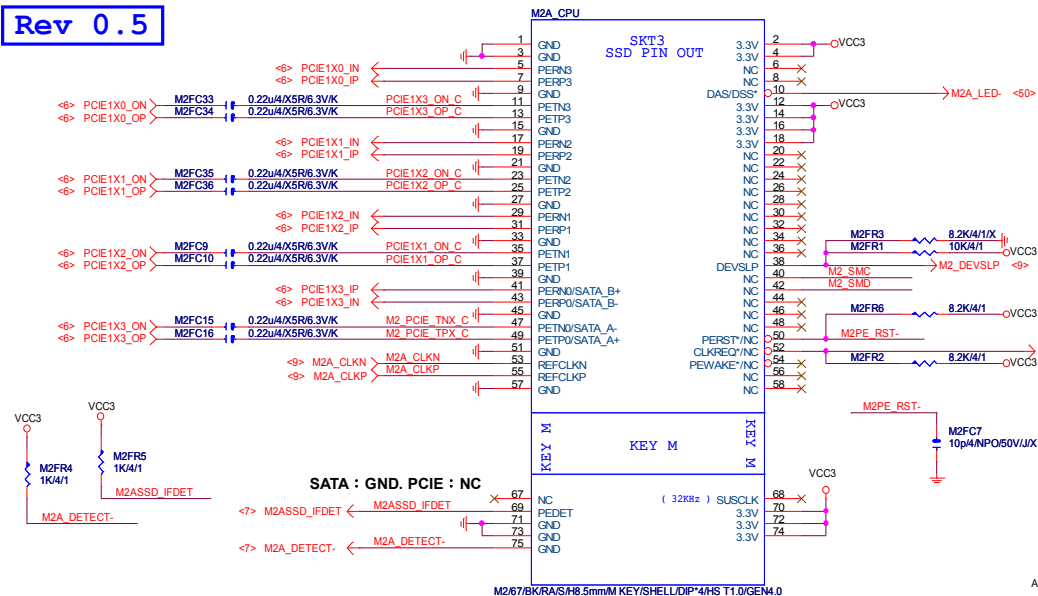
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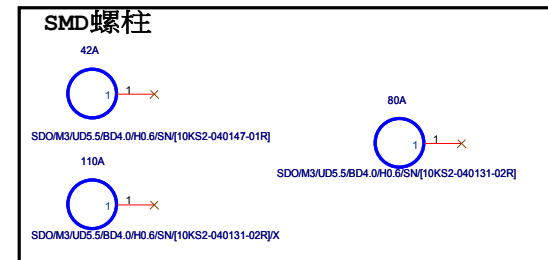
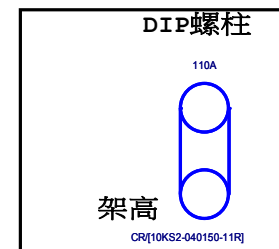
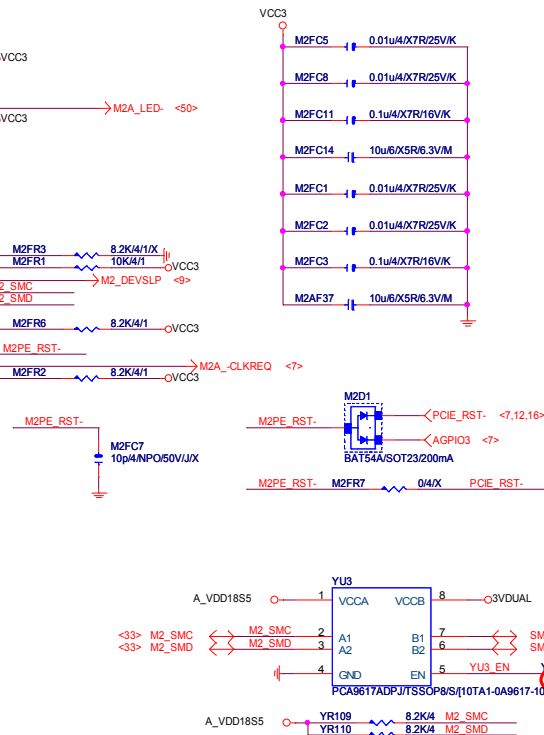
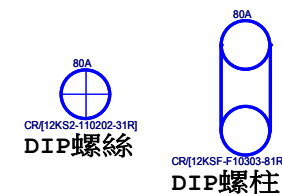


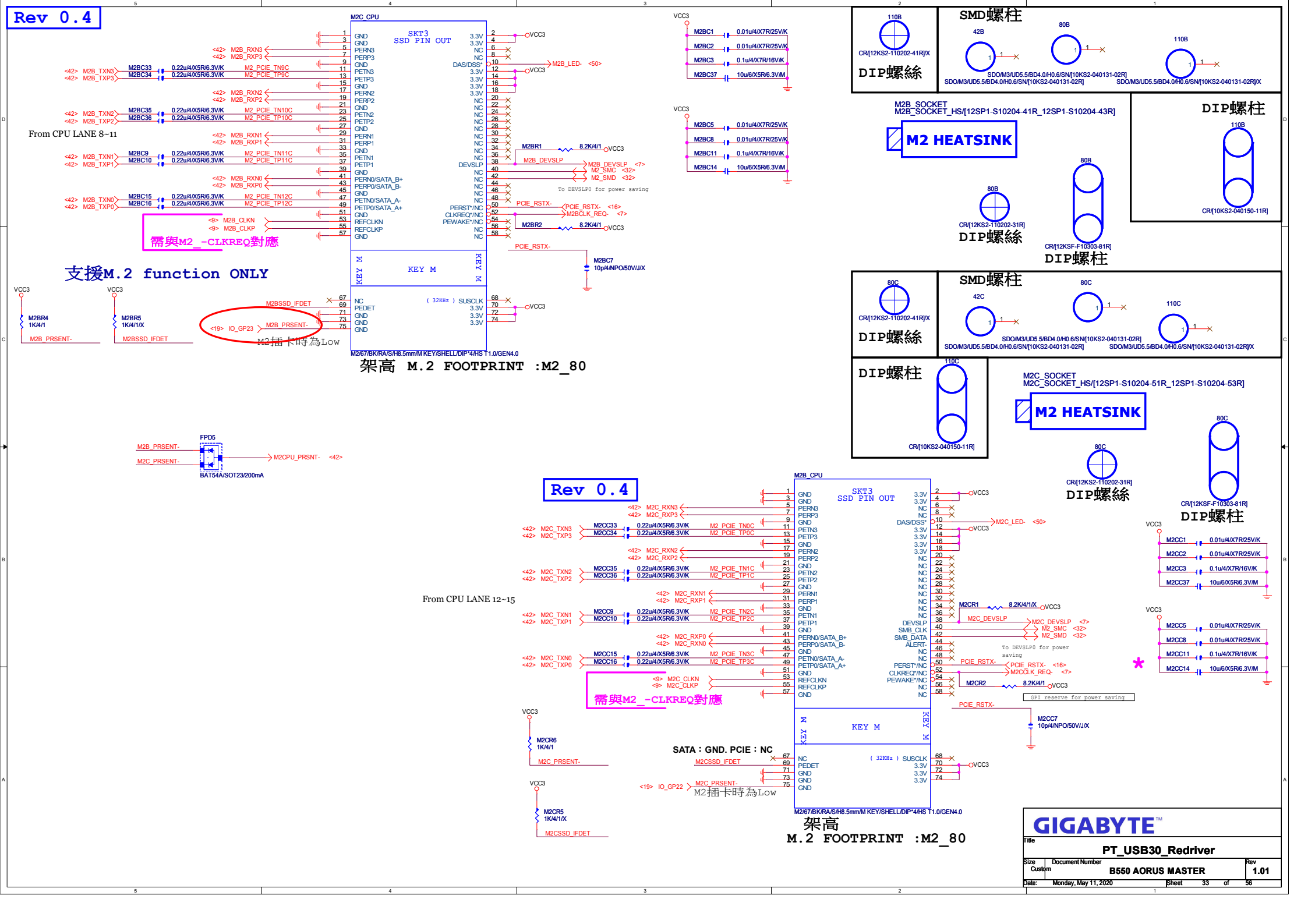


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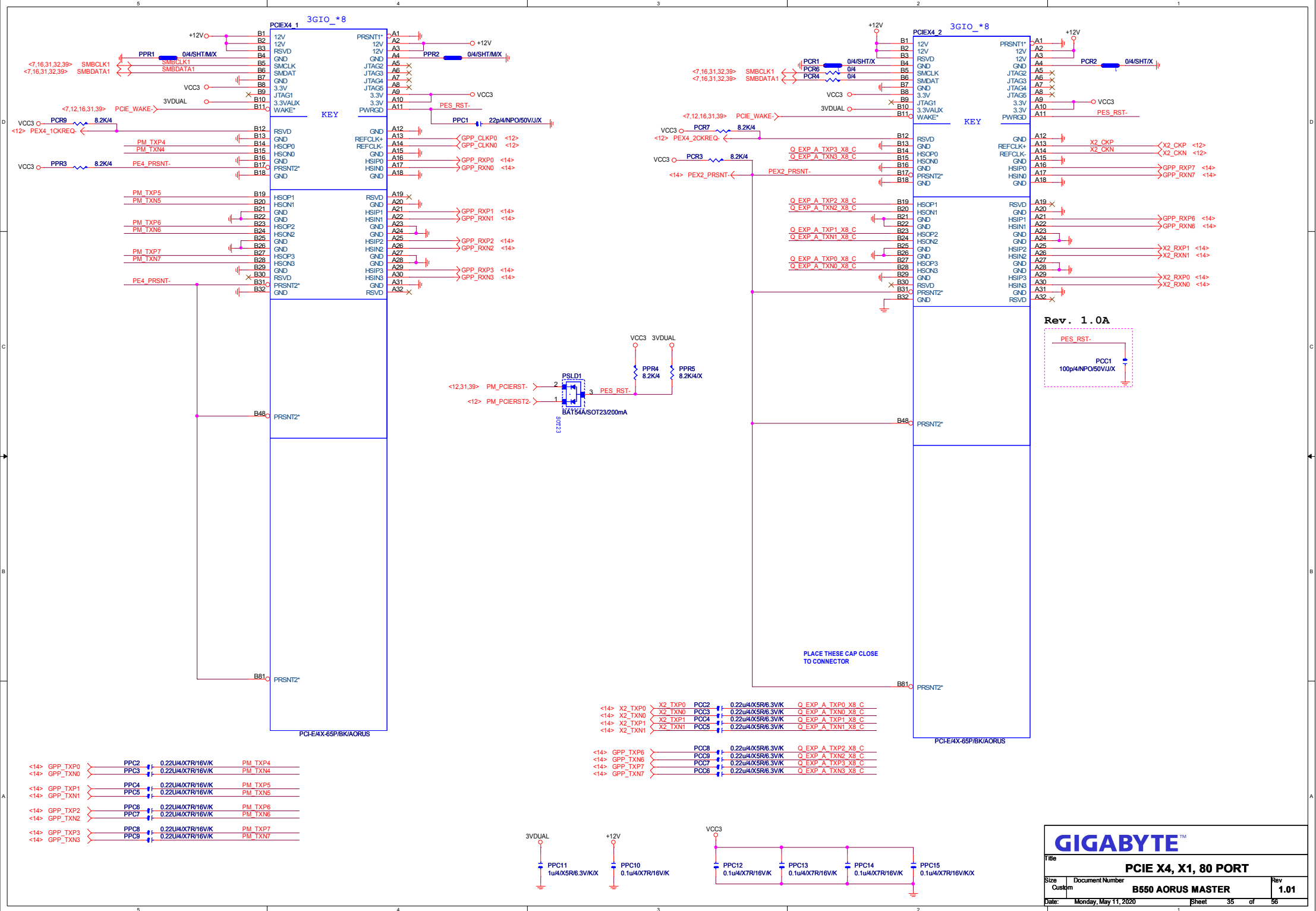
8.5H鐵殼
Footprint :M2_110(DIP)

M2A_SOCKET
M2A_SOCKET_HS[12SP1-S10204-31R_12SP1-S10204-33R]

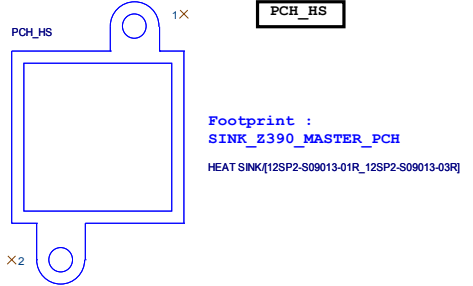
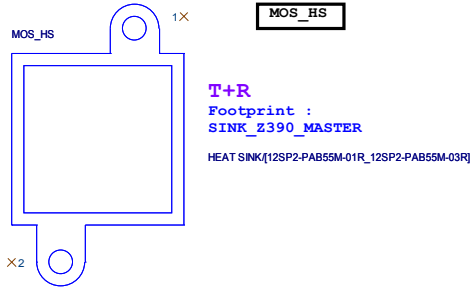
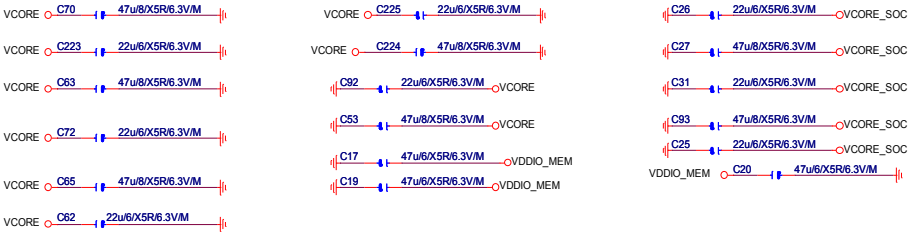




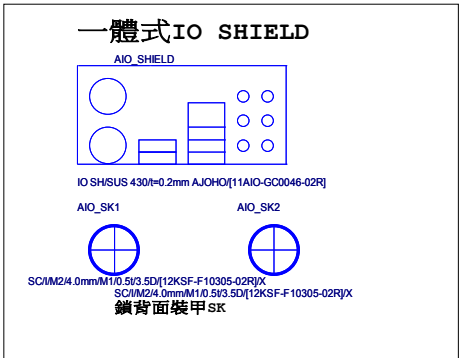
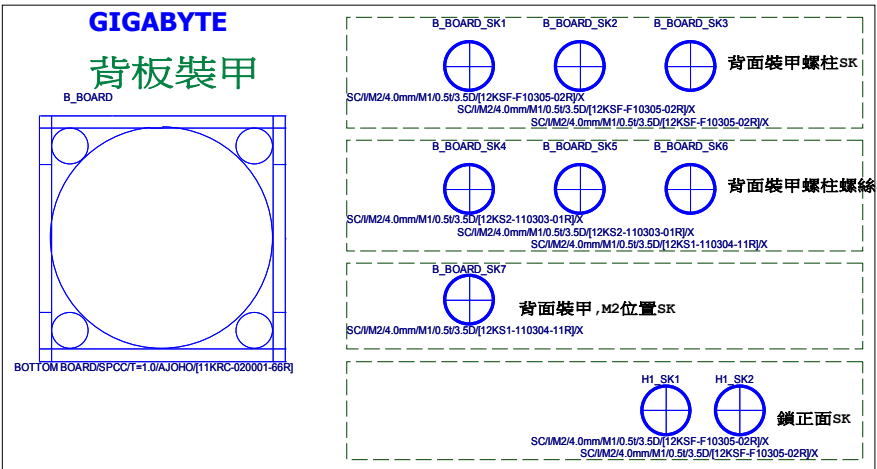
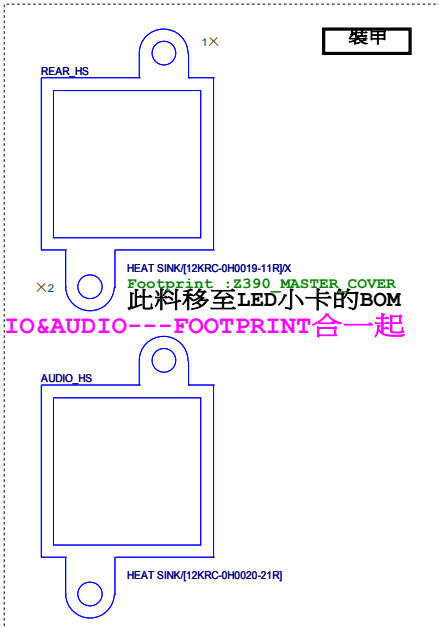
GIGABYTE TM			
Title KB_USB_DEC PWR			
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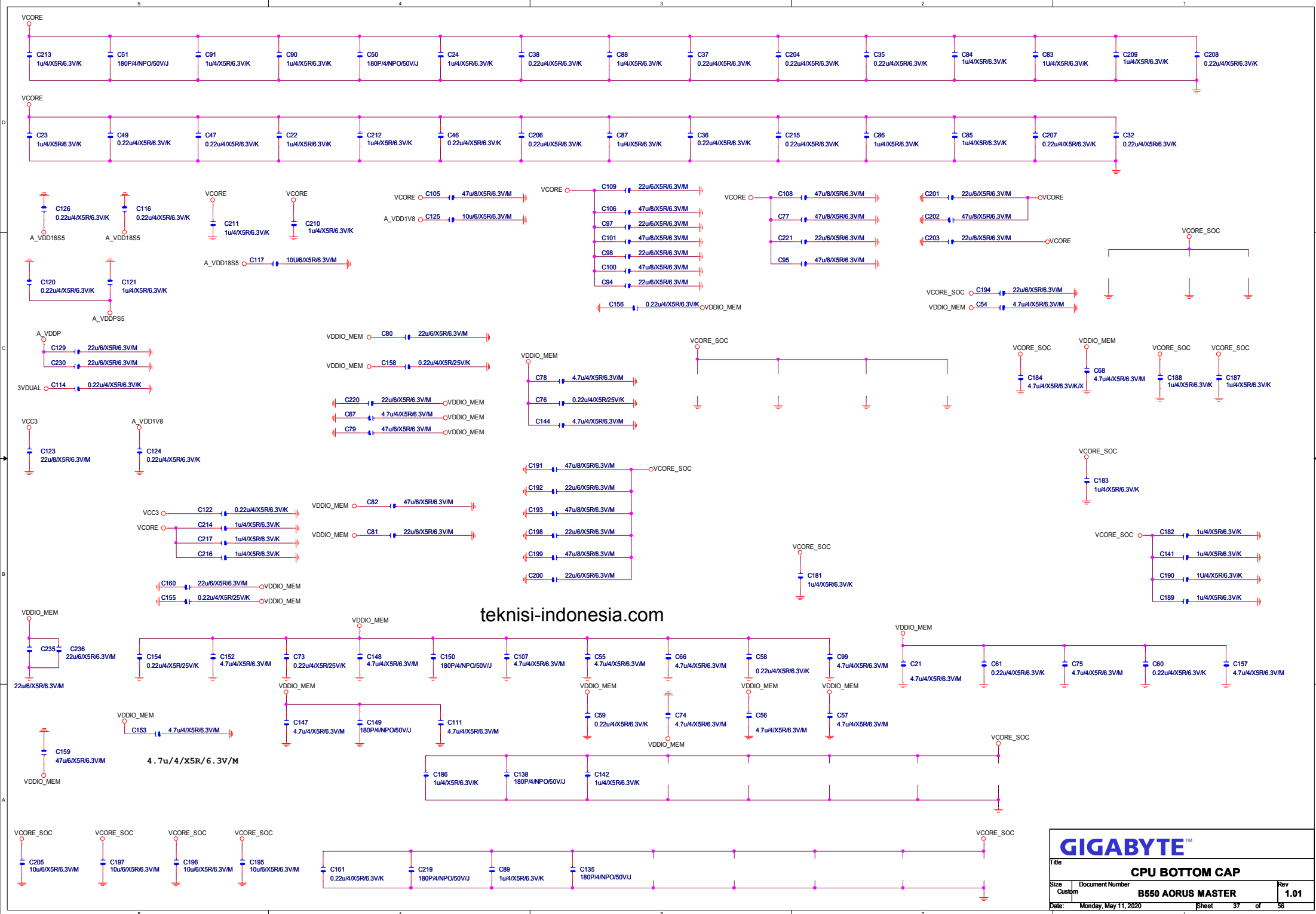
CPU TOP CAVITY



裝甲HEATSINK 分成四大部份

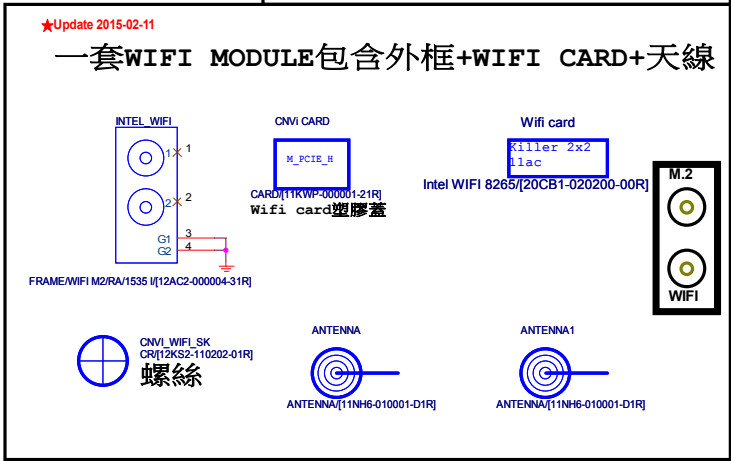
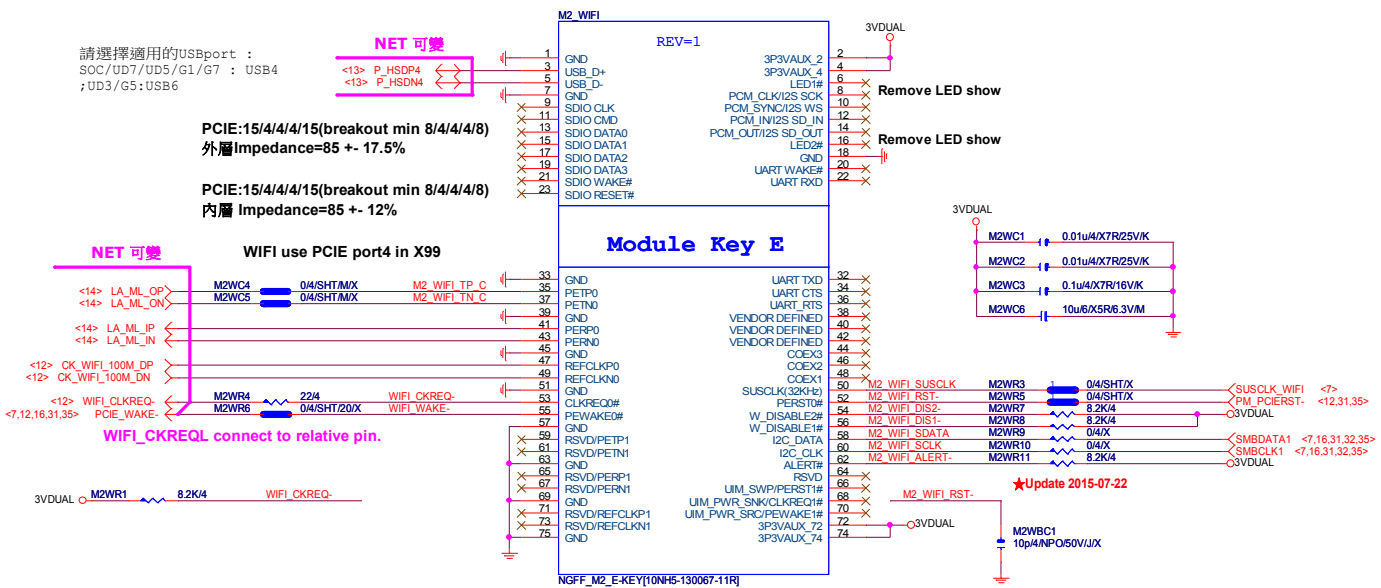


GIGABYTE™			
Title CPU TOP CAP			
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FOR M.2 WIFI MODULE @ REAR PANEL



Footprint Notice.

★Update 2015-07-22

★Footprint for
直立式 SMD:
WIFI-EKEY

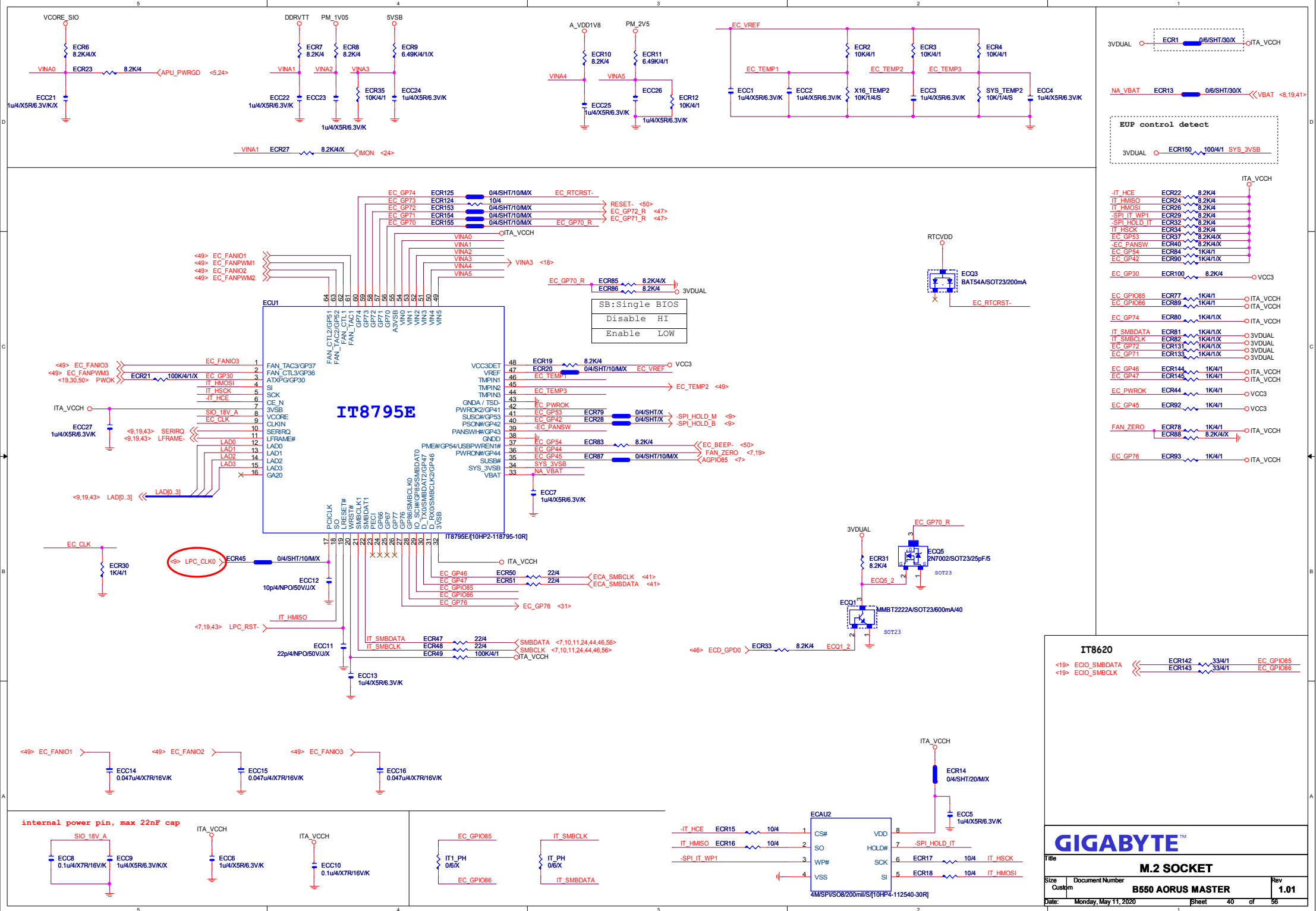
Footprint Notice.

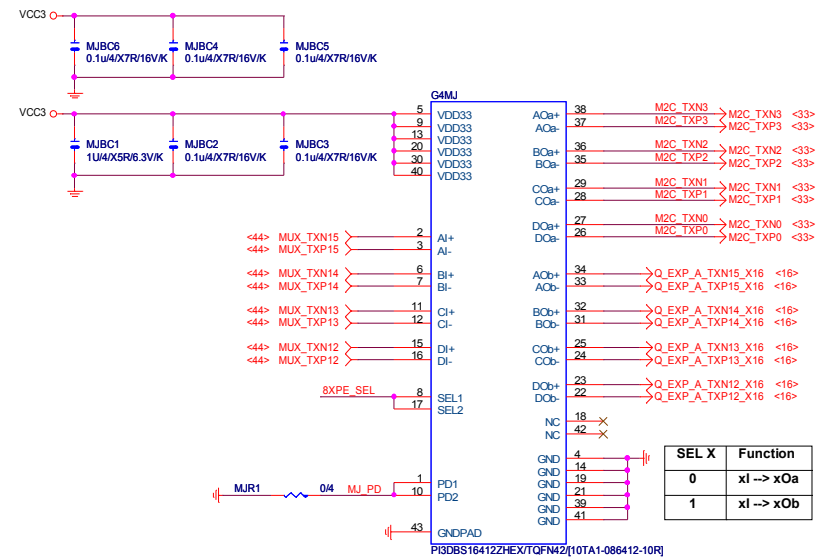
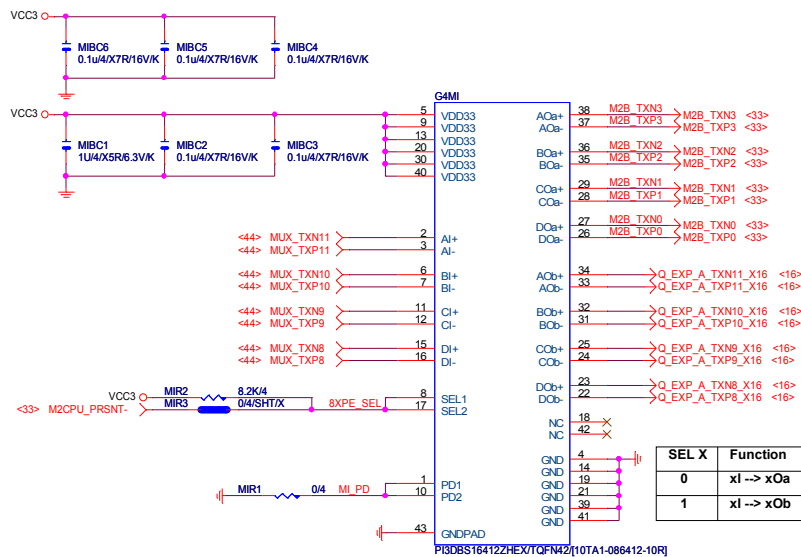
★Update 2015-07-22

★Footprint for 橫躺式 SMD:
NGFF-E-75P-2

GIGABYTE

Title			
M.2/U.2 SWITCH			
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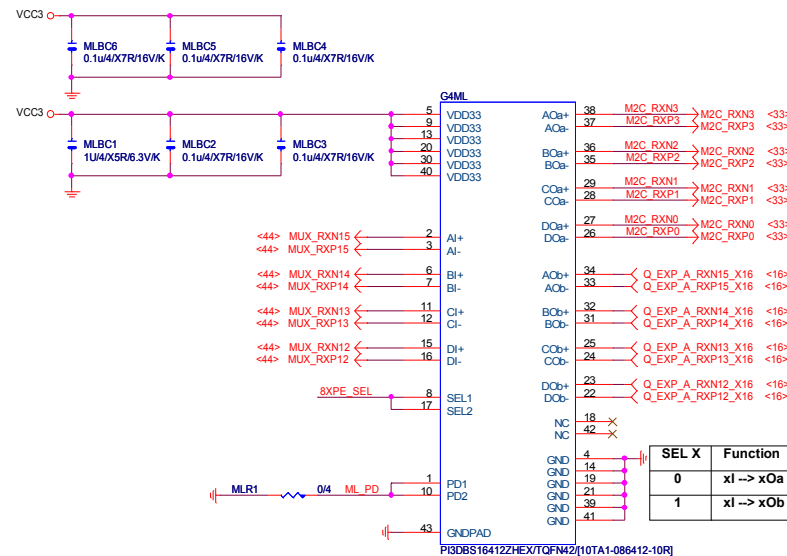
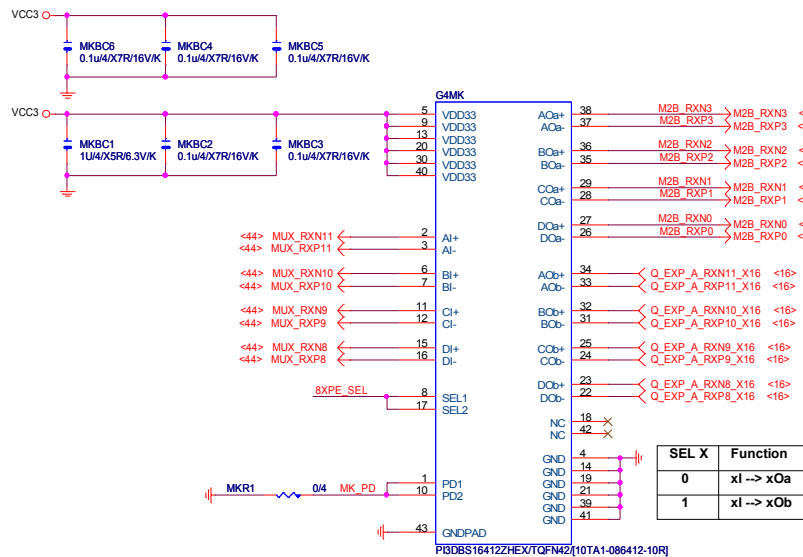


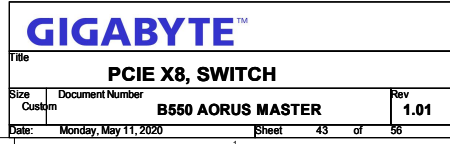
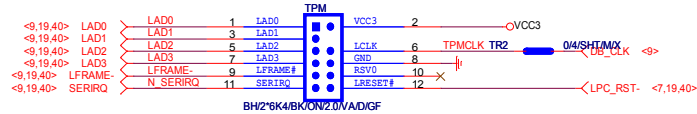
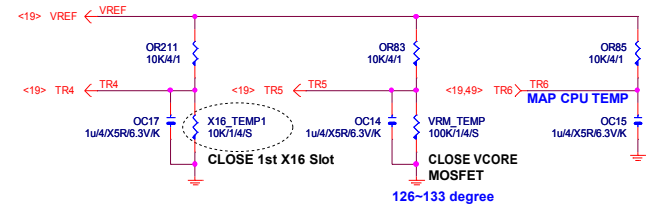


EXP_A_RXP[8..15] >>> EXP_A_RXP[8..15] <6,44>
EXP_A_RXN[8..15] >>> EXP_A_RXN[8..15] <6,44>

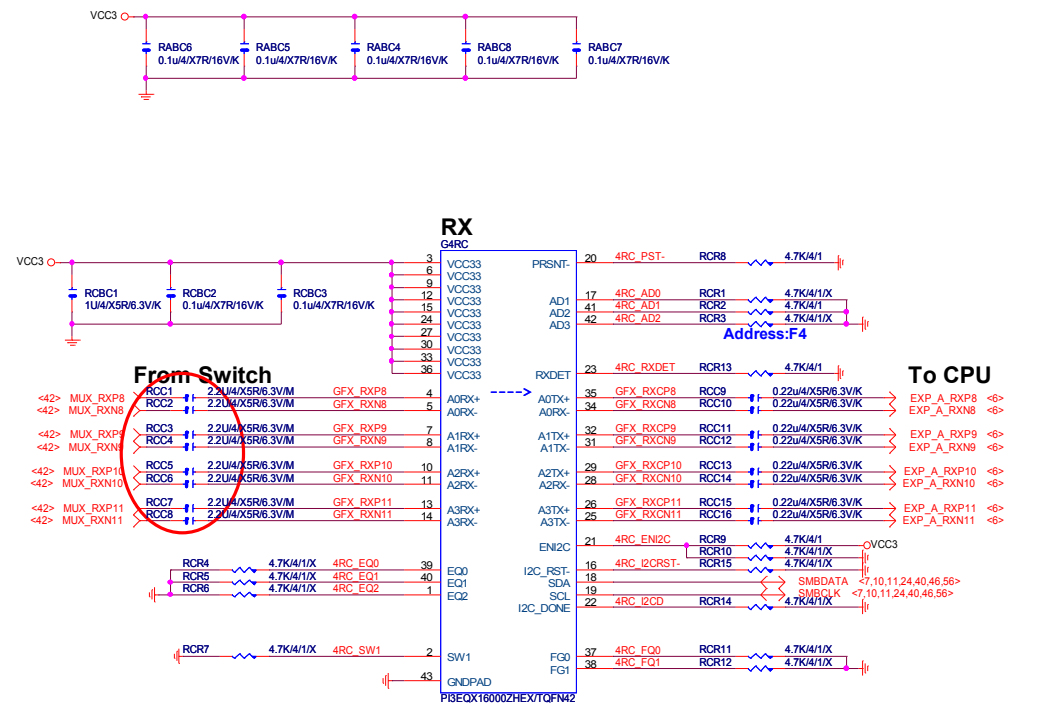
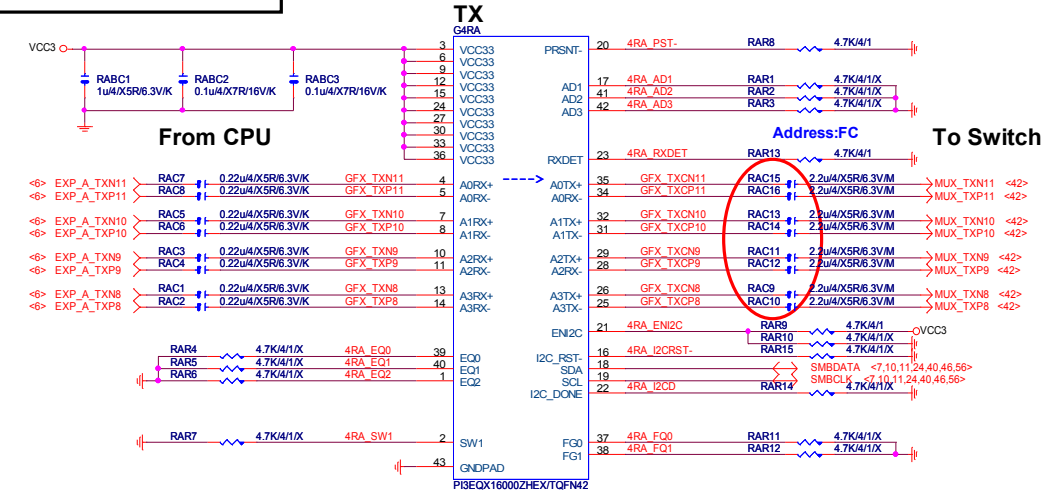
<6,44> EXP_A_TXP[8..15] >>> EXP_A_TXP[8..15]
<6,44> EXP_A_TXN[8..15] >>> EXP_A_TXN[8..15]

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PCIe GEN 4 REDRIVER



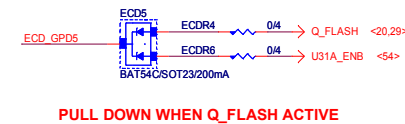
GIGABYTE™

Title			DIGITAL LED		
Size	Document Number	B550 AORUS MASTER			Rev
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GIGABYTETM

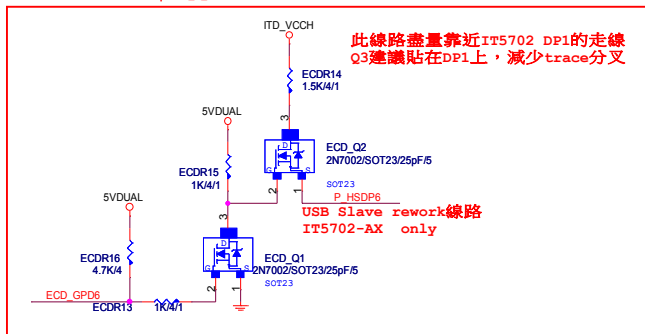
Title			ASM 2142 U31		
Size	Custom	Document Number	B550 AORUS MASTER		Rev
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Q-Flash Power Sequence

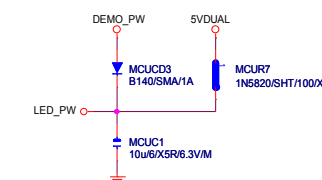
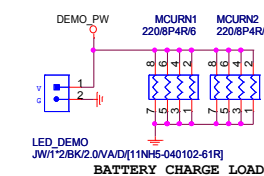
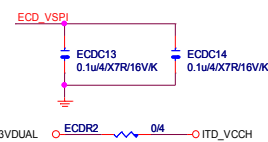
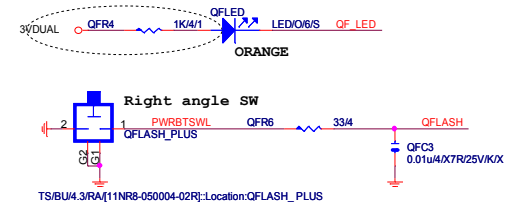
GPD0 pull-up to 3VSB
To ignore the test mode

PULL DOWN WHEN Q_FLASH ACTIVE:Disable Dual BIOS



此線路盡量靠近IT5702 DP1的走線
Q3建議貼在DP1上，減少trace分叉

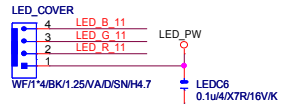
Q_FLASH BUTTON/LED



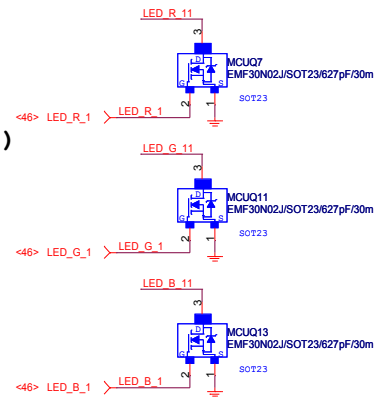
第一區 LED

第一區 LED CONTROL

FOR 後窗裝甲 led connect
(LED_COVER放在後窗裝甲內)



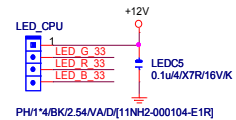
*Footprint : LED-1X4-1P25MM



第三區 LED

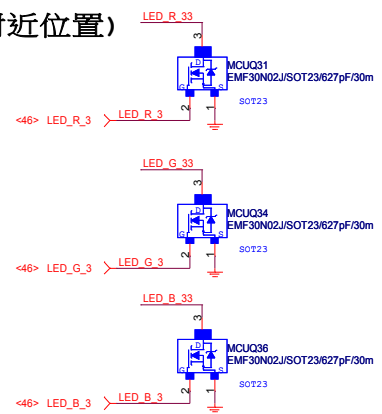
第三區 LED CONTROL

燈條 LED (LED_CPU放在CPU附近位置)



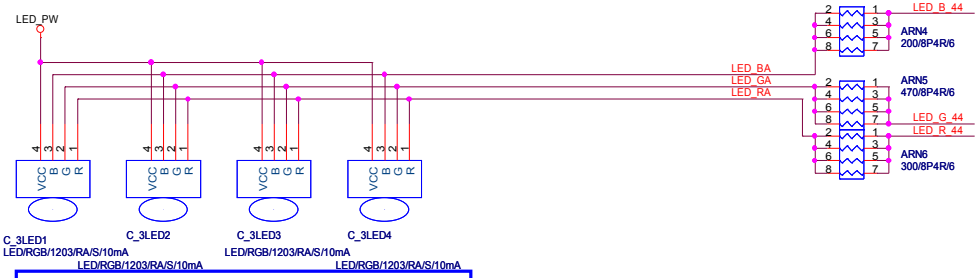
Footprint "PH1X4-FAN-AMD-L"

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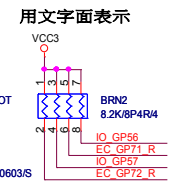
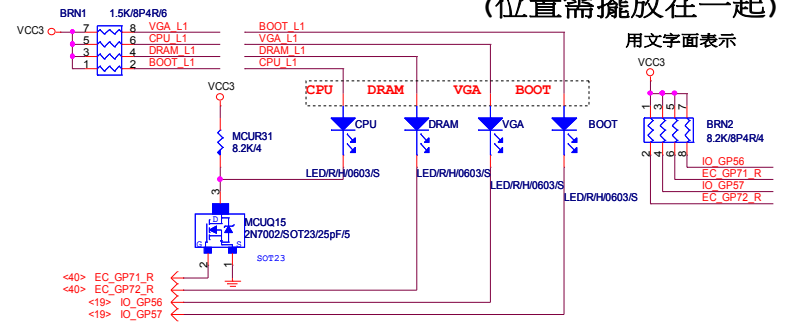
第四區 LED

FOR AUDIO 正板測發光 LED*4 (位置在正板,依據AUDIO_HS設計擺放)



FOOTPRINT: LED-4P-RGB-SIDE-1

DEBUG PORT LED *4 (位置需擺放在一起)

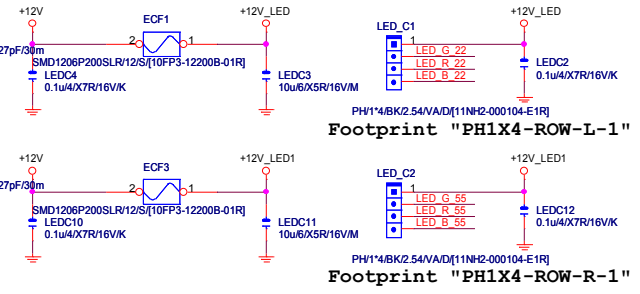
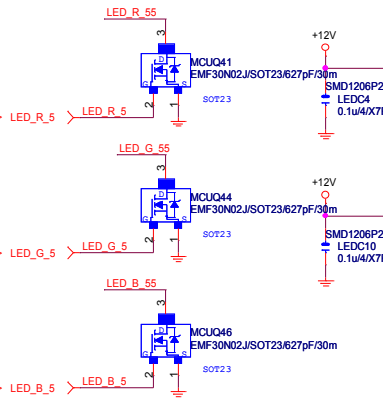
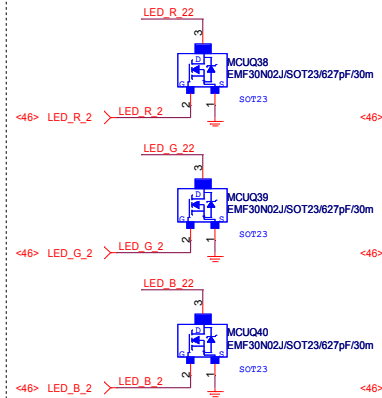


第五區 LED

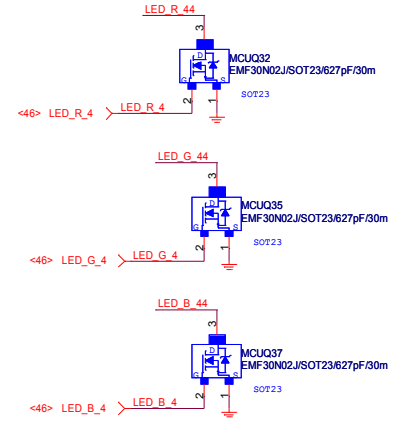
第二區 LED CONTROL

第五區 LED CONTROL

燈條 LED (LED_C1放在PCB左邊板邊位置)
燈條 LED (LED_C2放在PCB右邊板邊位置)

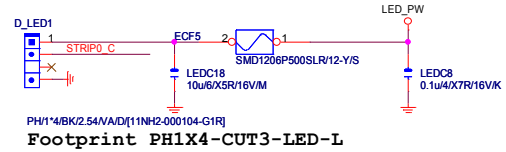


第四區 LED CONTROL



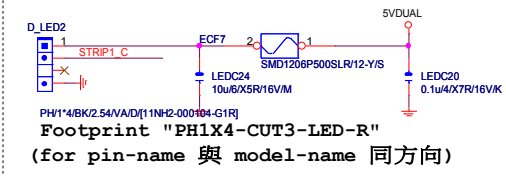
第六區 LED (靠近左上板邊位置)

Digital LED Strip1

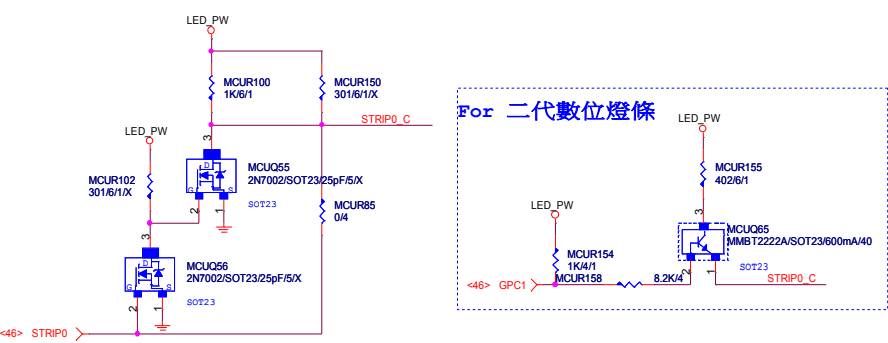


第七區 (靠近右下CPU板邊位置)

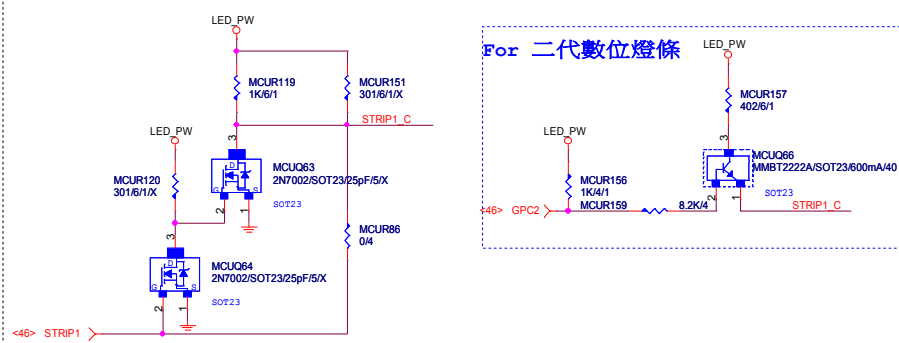
Digital LED Strip2



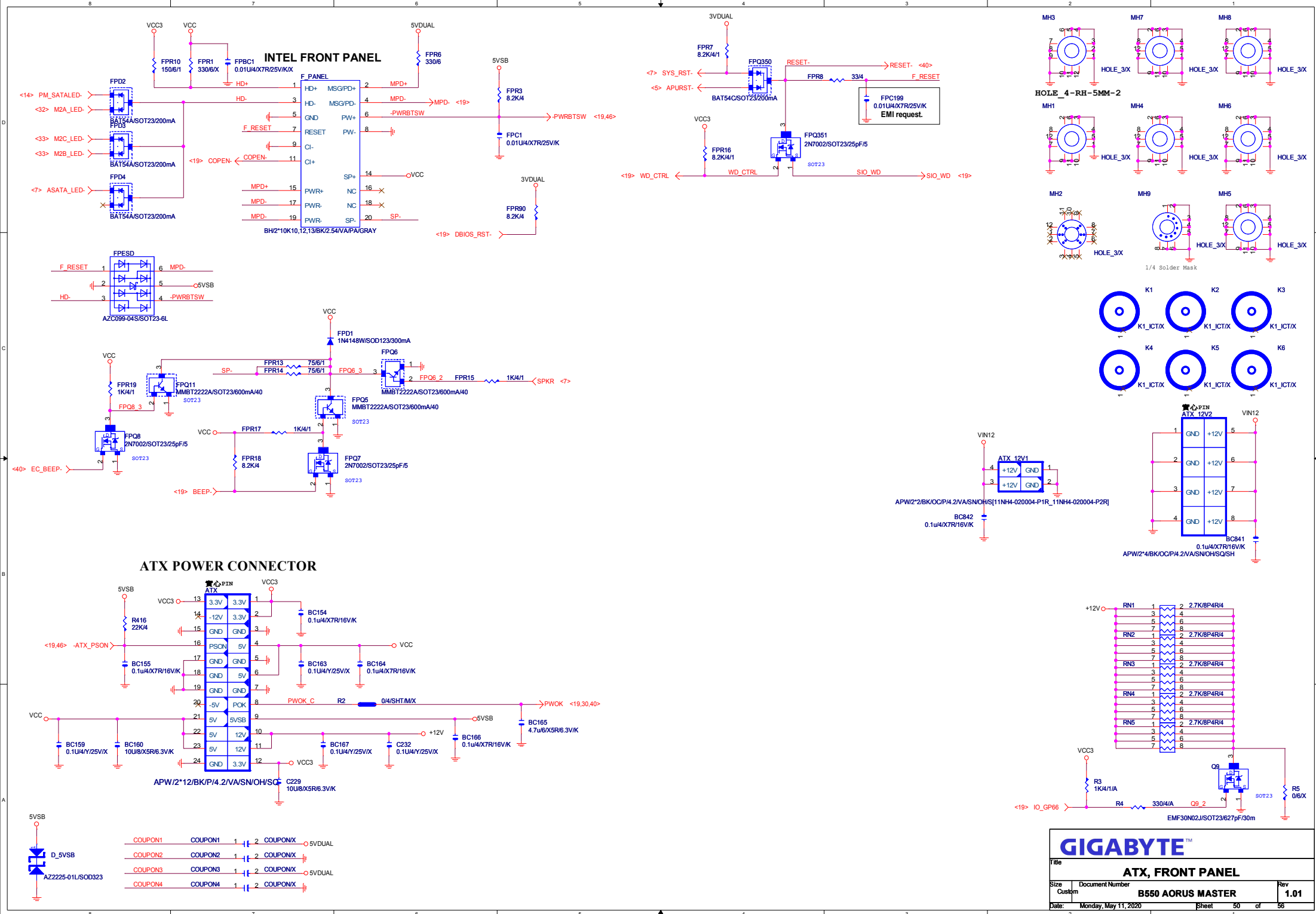
燈條 Level shift



燈條 Level shift





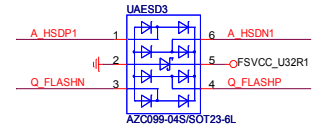
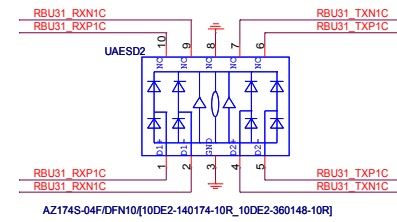
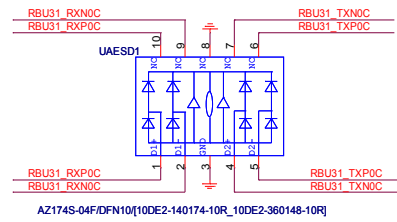
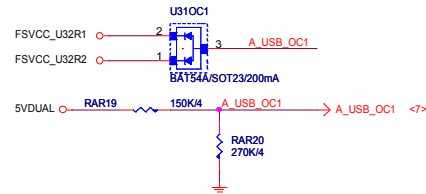
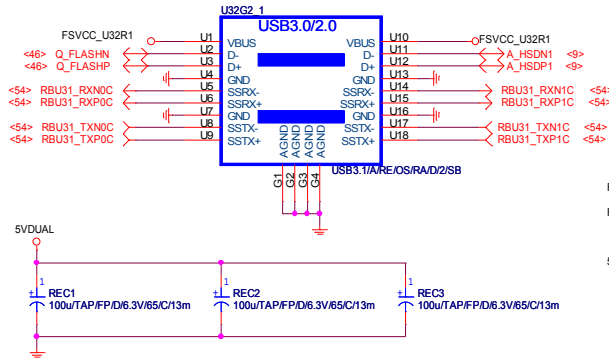




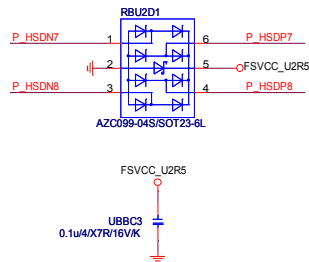
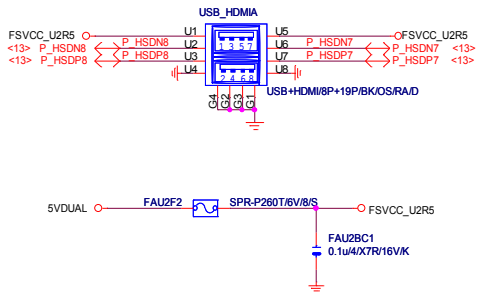
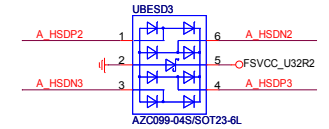
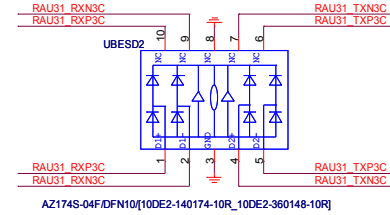
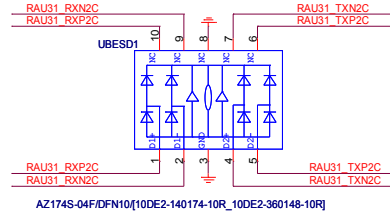
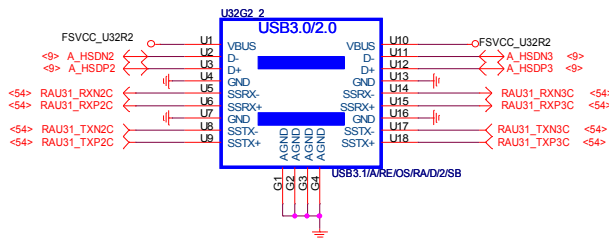
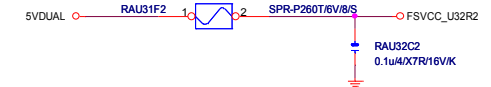
GIGABYTE TM			
Title Realtek RTL8125			
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R_USB30 PORT



CONNECTOR料號要改



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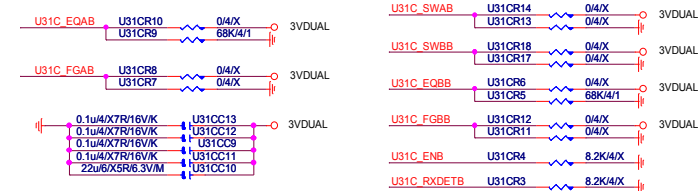


Figure 10 shows the recommended component values for the 3V dual inductor power supply. The components are organized into two columns, each connected to a 3VDUAL supply.

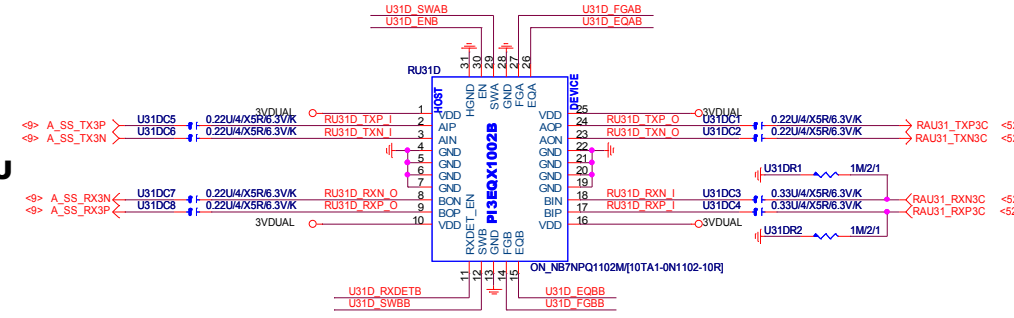
Left Column Components:

- U31D_EQAB:** Connected to U31DR10 and U31DR9 through a 04/X capacitor and a 68K/4/1 inductor.
- U31D_FGAB:** Connected to U31DR8 and U31DR7 through a 04/X capacitor and a 04/X inductor.
- Capacitor Network:** A series of four 0.1uF/X7R/16V/K capacitors and one 22uF/X5R/3V/M capacitor are connected to the 3VDUAL supply.
- Inductor Network:** A series of four inductors (U31DC13, U31DC12, U31DC11, U31DC10) are connected to the 3VDUAL supply.

Right Column Components:

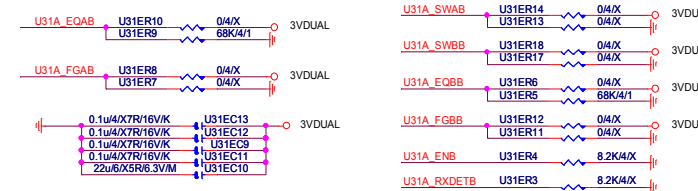
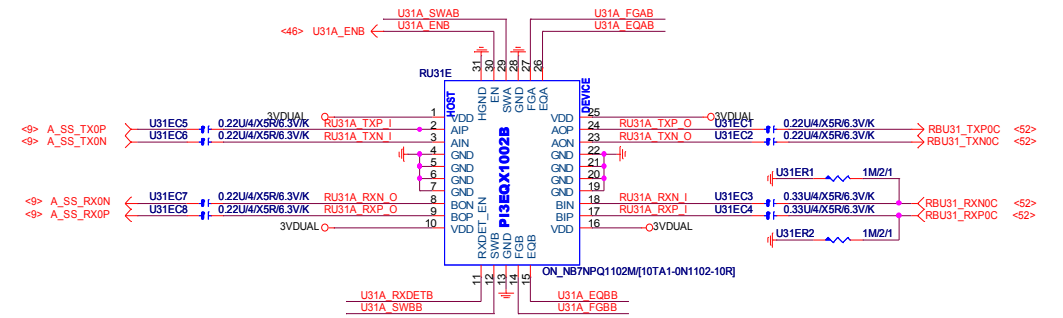
- U31D_SWAB:** Connected to U31DR14 and U31DR13 through a 04/X capacitor and a 04/X inductor.
- U31D_SWBB:** Connected to U31DR18 and U31DR17 through a 04/X capacitor and a 04/X inductor.
- U31D_EQBB:** Connected to U31DR6 and U31DR5 through a 04/X capacitor and a 68K/4/1 inductor.
- U31D_FGBB:** Connected to U31DR12 and U31DR11 through a 04/X capacitor and a 04/X inductor.
- U31D_ENB:** Connected to U31DR4 through an 8.2K/4/X resistor.
- U31D_RXDETBB:** Connected to U31DR3 through an 8.2K/4/X resistor.

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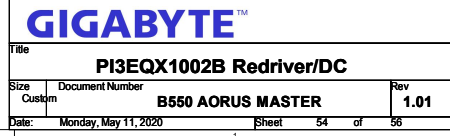
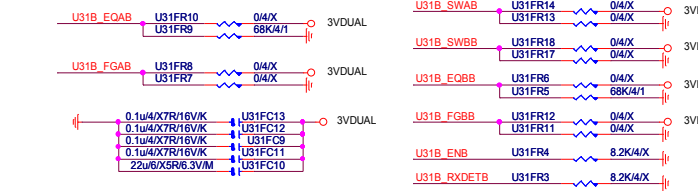
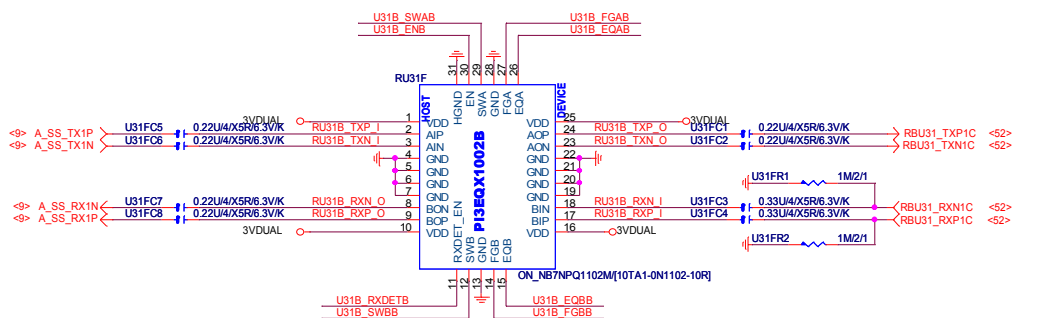


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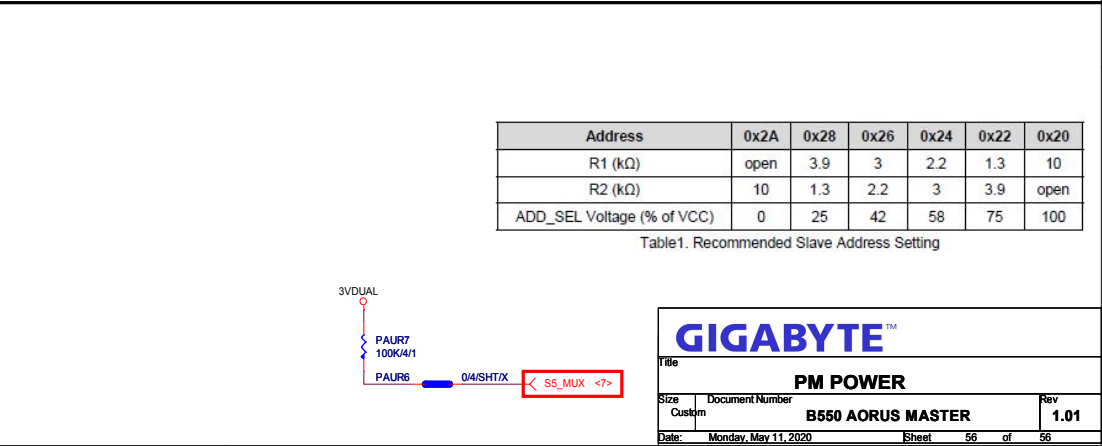
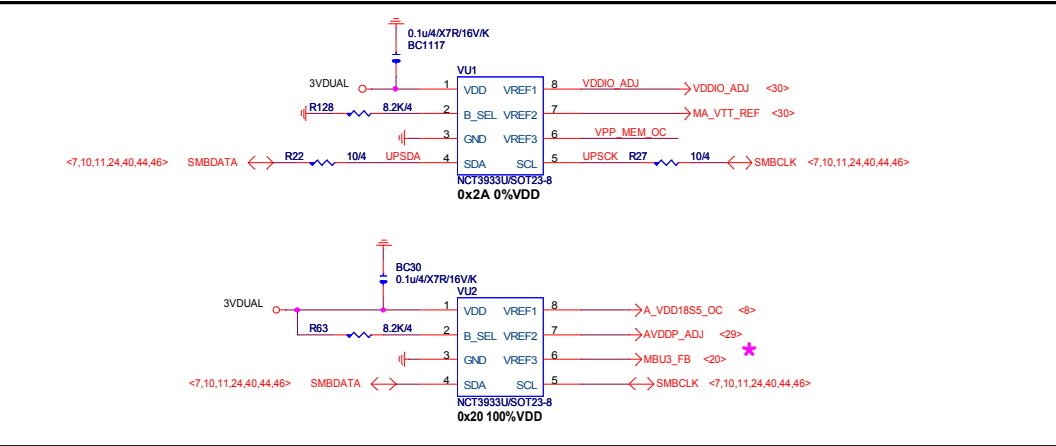
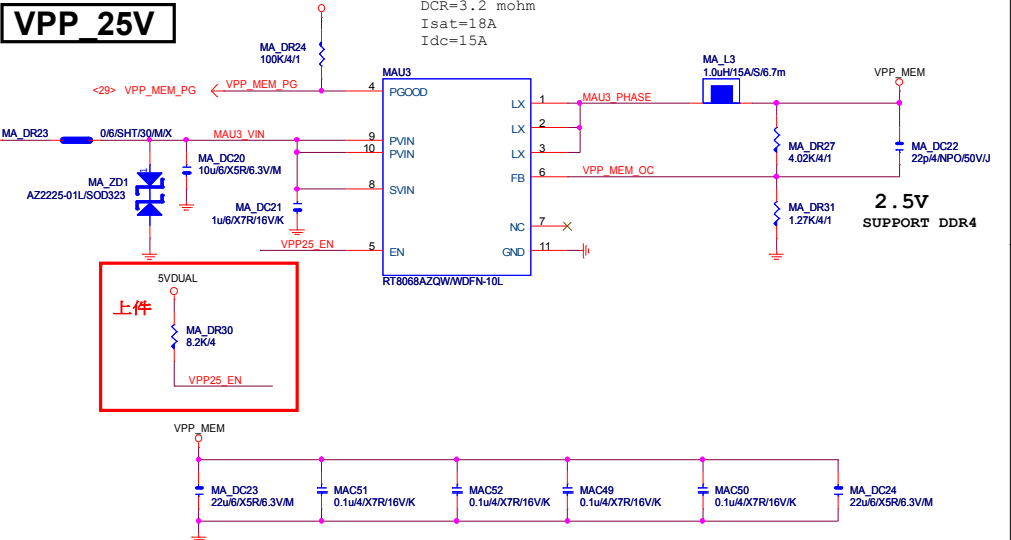
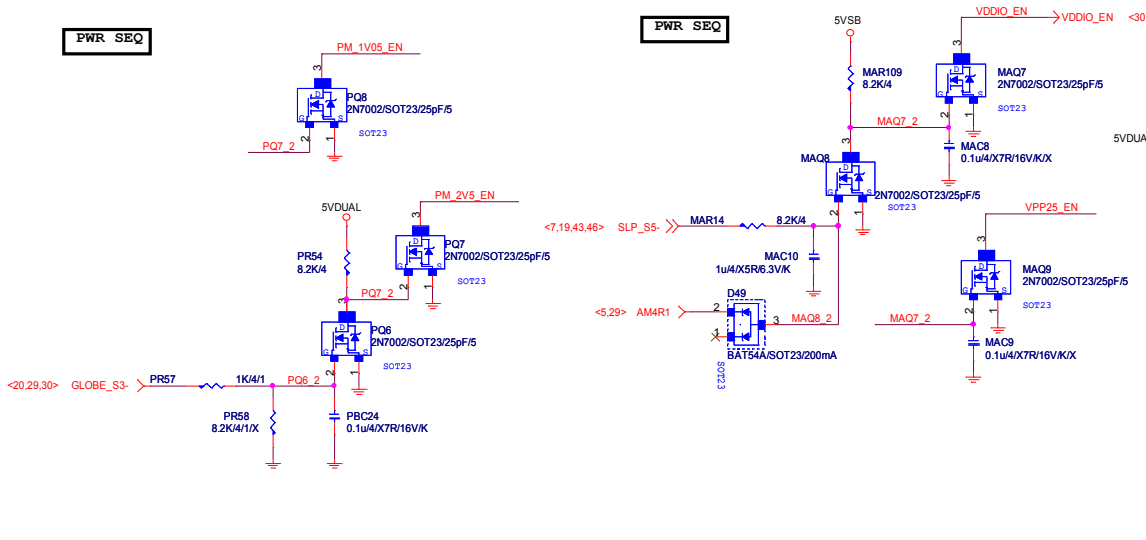
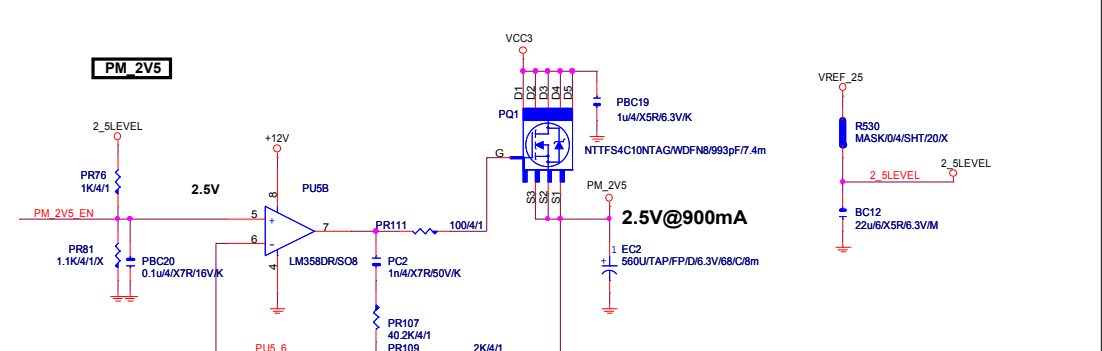
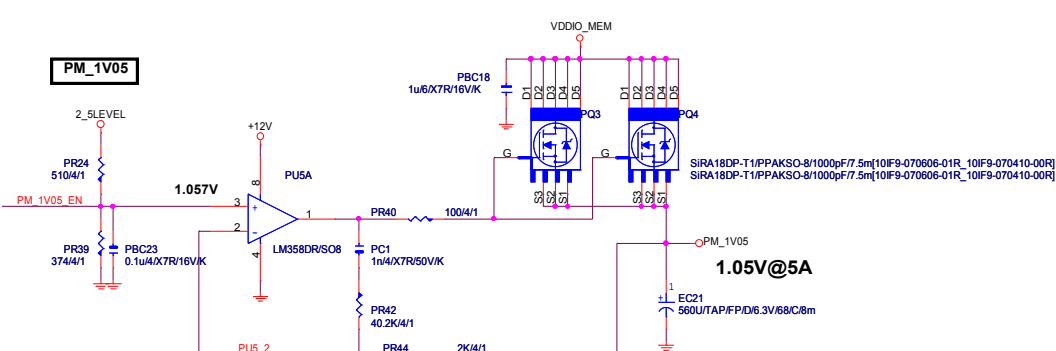


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X570 POWER			
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Address	0x2A	0x28	0x26	0x24	0x22	0x20
R1 (kΩ)	open	3.9	3	2.2	1.3	10
R2 (kΩ)	10	1.3	2.2	3	3.9	open
ADD_SEL Voltage (% of VCC)	0	25	42	58	75	100

Table1. Recommended Slave Address Setting

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